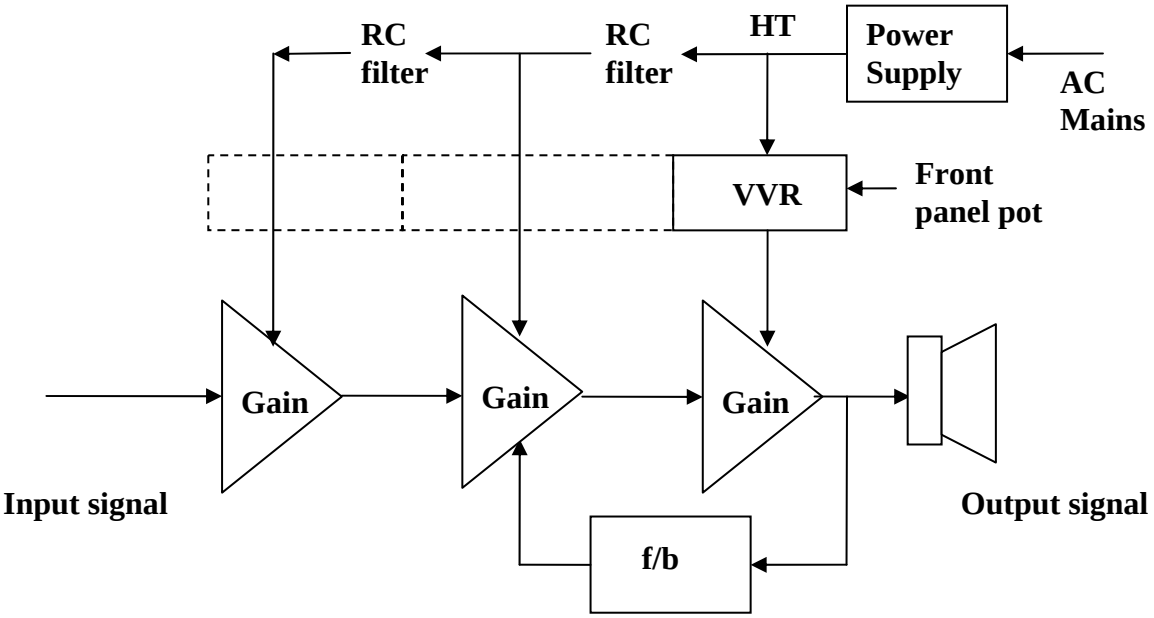
Variable Voltage Regulator Information

The aim of a Variable Voltage Regulator (VVR) is to make an amplifier sound as if it is cranked without having a correspondingly high output signal level at the speaker. This is achieved by lowering the voltage in the HT feed to an amplifier circuit stage, with the voltage level at the amplifier stage made variable over a wide range by user control (ie. front panel pot).



Most amps and combos generate a pleasing sound character when the volume is raised to the point where overdrive and other higher level distortions become significant. But not everyone is enamoured by the sound levels of a cranked amp. With this in mind, an increasing number of amps are being modified to include VVR (also referred to as 'power scaling'). A variety of kits of parts are available, and the technique is well within reach of those who are happy to electrically modify an amp.

The more common technique to achieve the same result is the load attenuator ('power soak', 'hot plate' style), which doesn't change the amplifier at all but instead fully loads the amplifier with a constant resistance, and just passes an attenuated signal level through to the speaker.

You can find many discussions and diatribes on the web about using load attenuators and VVR circuits. Each of these techniques introduce a variety of compromises when compared to a standard setup, and I suggest one keeps an open mind about what can be achieved by installing a VVR circuit.

Like good amp design, VVR design and implementation covers many issues that are worth considering before changes are made with the soldering iron or drill bit. The VVR topic can become quite complex if a thorough appreciation is required, and so this article can only try to provide an introduction on the following main topics, and can only give examples for the purposes of illustration:

- VVR control
- Which stage(s) to include.
- VVR protection for over-voltage and over-current
- FET power dissipation

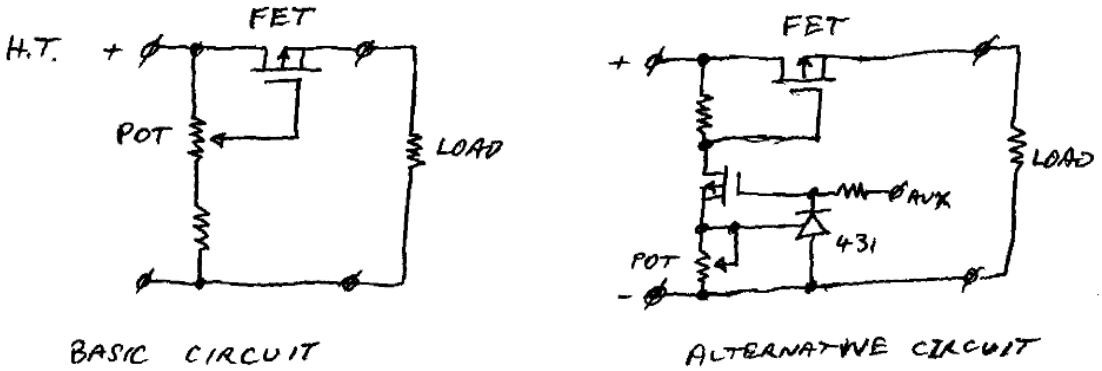
- Compromises
-Feedback

VVR control

The generic VVR circuit uses a power FET to drop a certain voltage between the amp's HT DC supply (after the rectifier diodes and initial filter components), and the supply line to the chosen amp stage(s). The VVR circuit has only a few parts, and can be mounted on a small circuit board along with the control pot - kit circuits are pretty similar, but can have a few differences in circuit design, protection and implementation. Some practical circuits are identified in the references.

A pot is used to control the voltage at the FET gate, and hence set the voltage presented to the stage. In most kit circuits, the pot can have a few hundred volts across its terminals, and the input terminal sits at the amp's HT level. Such DC levels may exceed pot voltage specifications, and may lead to creepage or insulation breakdown, especially from dirt build up over time, and typically requires the use of a physically large pot.

An alternative means of generating a voltage at the main FET gate is to use a constant current source for the lower leg of the voltage divider section (instead of the pot), with the upper leg being a normal resistor. By changing the current level in the lower leg, the voltage drop across the upper resistor varies. A constant current source for the lower leg can simply be made using a low power, high voltage FET with a source resistor acting as the current sense. The lower leg FET gate voltage is controlled by a shunt regulator (eg. npn transistor or TL431), which is turned on by the voltage drop across the current sense resistor in the source leg. The current sense resistor is the control pot. The supply for the FET's gate bias voltage is from a separate auxiliary supply, or dropped from the HT. The control pot operates at a low DC voltage level. The following simplified schematics indicate the technique.



This technique also allows multiple main FETs, placed in series, to equally share the dropped voltage between the HT supply and the amp stage, and for these FETs to be controlled with a single pot. And this technique also provides a convenient point to interface other control signals, if needed.

Which stage(s) to include

VVR can be used to lower the HT supply levels to all stages of an amplifier. This can be thought of simply as using a variac to control the input AC mains voltage (but somehow keeping the heater voltage at the correct level). Some people prefer this method, and it should be simple to implement with a kit, and should allow all the volume/gain controls to operate as per normal. However most amplifiers have a number of gain and effect stages, and the impact of lowering

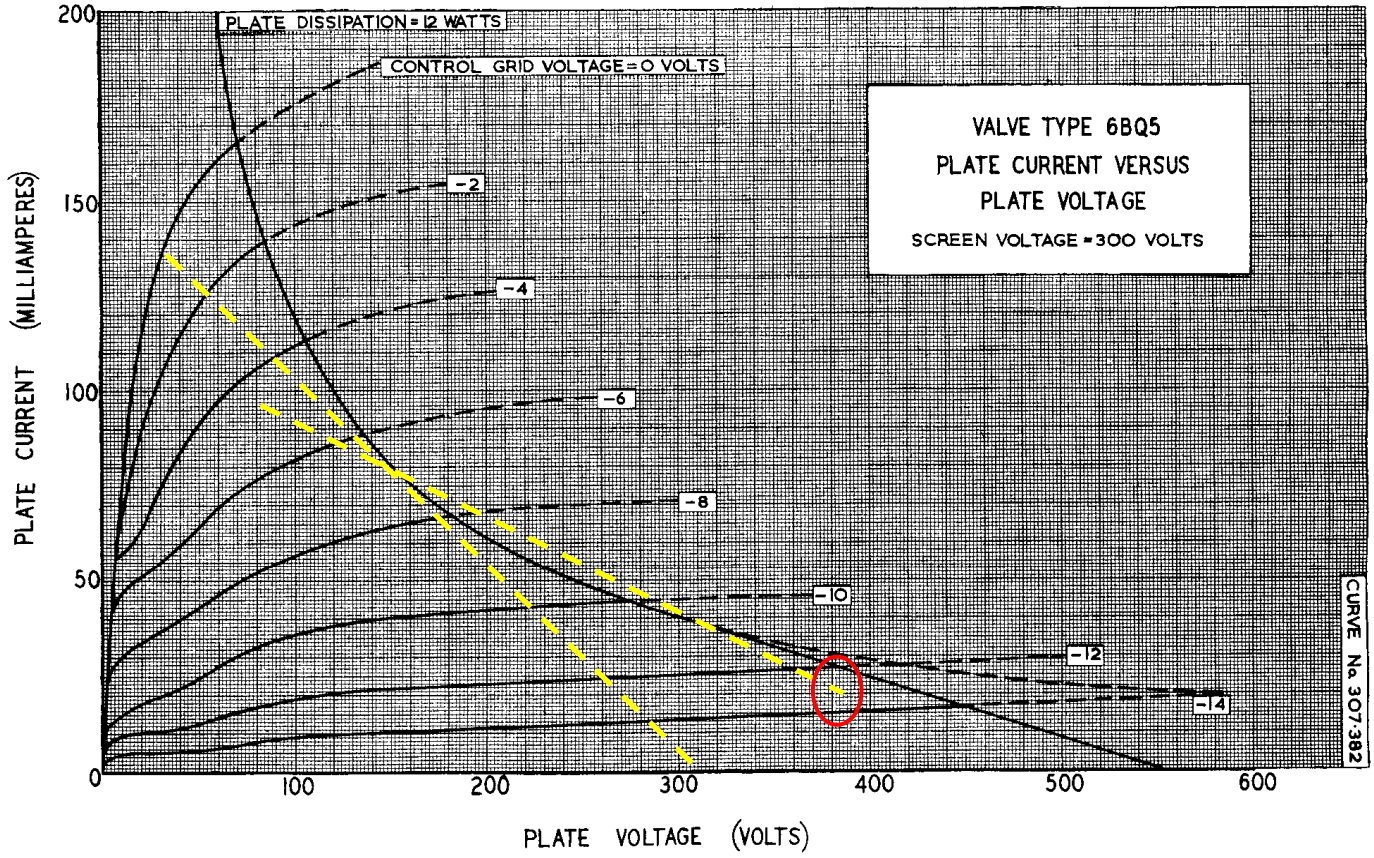
the HT voltage to all stages may not be simple to appreciate. Trying to describe the implications to each stage is beyond this article.

Another simple configuration is to lower the supply voltage to just the output stage, or the PI and output stage. This article is limited to just describing VVR used with a cathode biased Pentode PP output stage where the screen supply is derived directly from the anode supply voltage (ie. the OPT centre-tap voltage). In this simple case, the intent would be for the other stages to operate under normal supply voltage conditions, with the idle supply voltage to the PI and preamp stages remaining close to the original levels. This simple case comes with a set of compromises, with the main one being that the previous stages will overdrive the output stage as the VVR drops the voltage to the output stage more.

VVR Design Example for cathode biased pentode PP output stage

To get into the thick of the impact on design, the following description is based on an EL84/6BQ5 pentode PP output stage with cathode biasing. The impact of voltage sag is also included, as it is typically a significant effect in guitar amps.

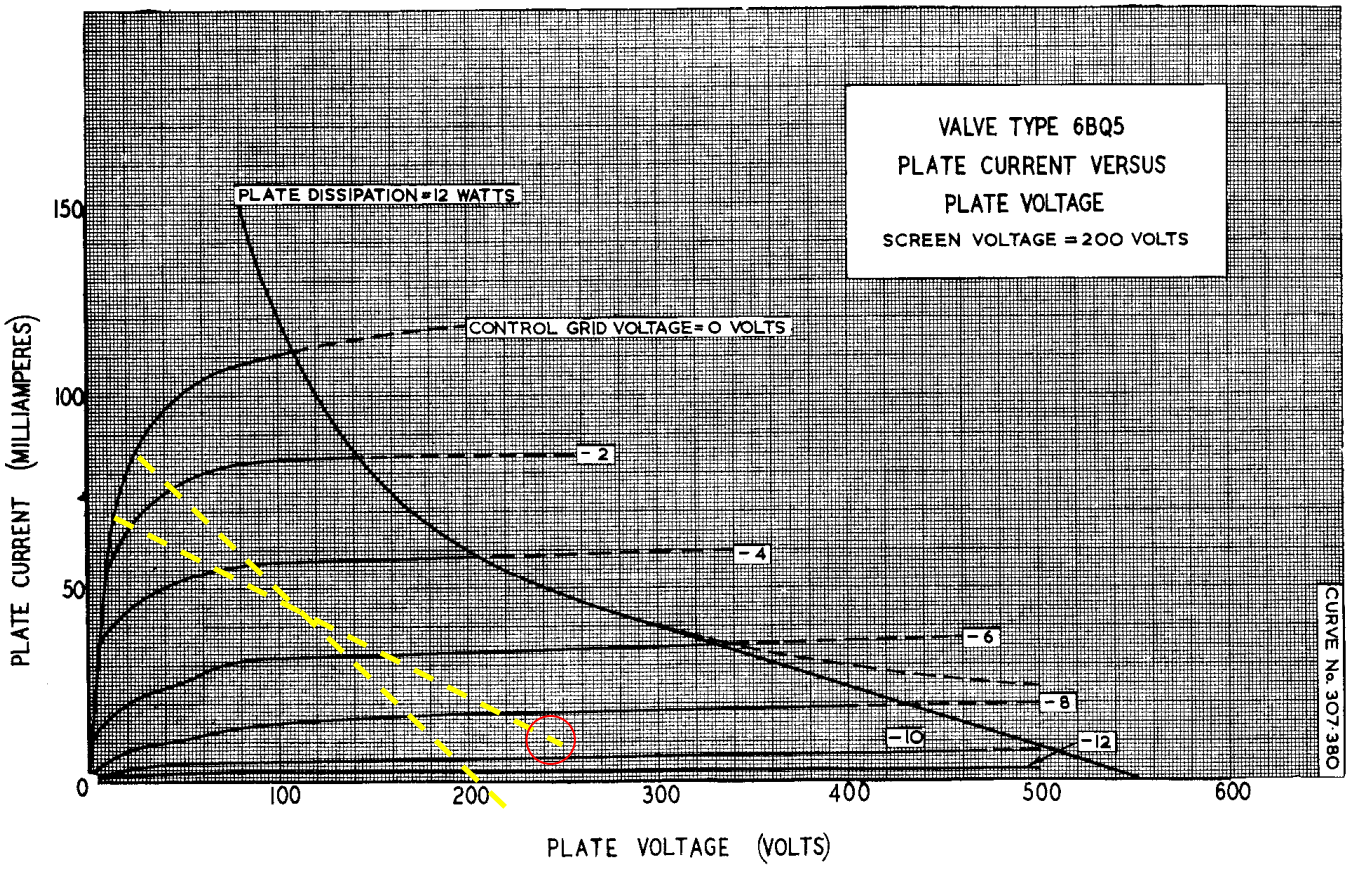
The example output stage has an idle supply voltage of 400V to the anodes and screens, sagging to about 300V at full loading. An 8kΩ plate-to-plate OPT presents signal currents into each tube with a 4kΩ load impedance with both tubes conducting, reducing to 2kΩ load impedance at higher levels. Cathode bias is set to 20mA at idle (grid bias voltage about 18V as screen voltage is close to 400V). An unmodified (non VVR) loadline graph for this output stage is shown below using default characteristic curves when the screen is 300V.



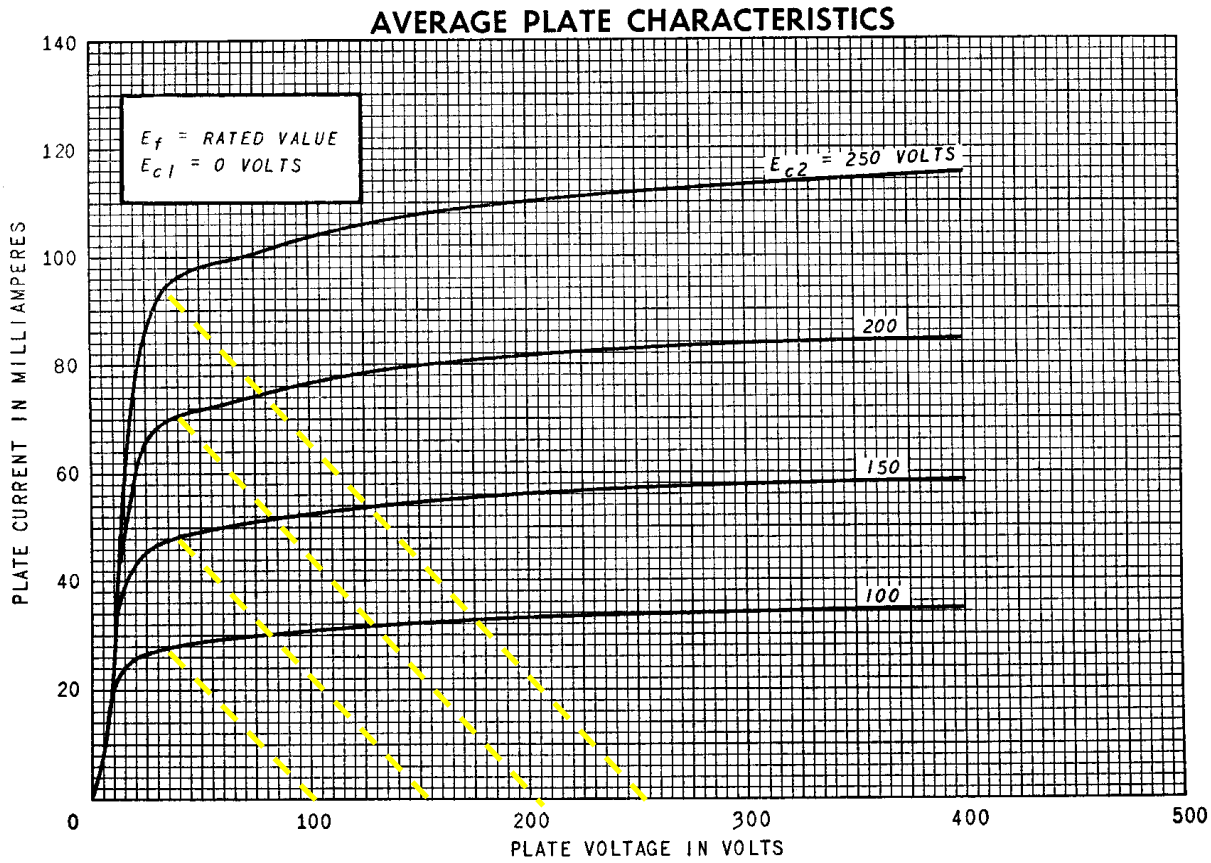
Now if we use VVR to reduce the idle voltage down to say 250V, then the loadline looks like the following graphic, which uses characteristic curves for screen voltage of 200V. Note that sagging of the HT voltage is less in this case as signal levels are lower, so the loadline assumes a sagged voltage level of 200V is available for high loads. Loading impedances don't change.

With no change to cathode bias resistor values the cathode bias current is reduced at idle, as screen voltage is closer to 250V. Note that the loadline still extends into the same general knee zone for peak levels, and is likely to exhibit similar compression distortion going in to overdrive (although the compromise is that the voltage sag on anode and cathode is not as pronounced). Also note that idle voltages to other stages may rise if output stage bias current drops.

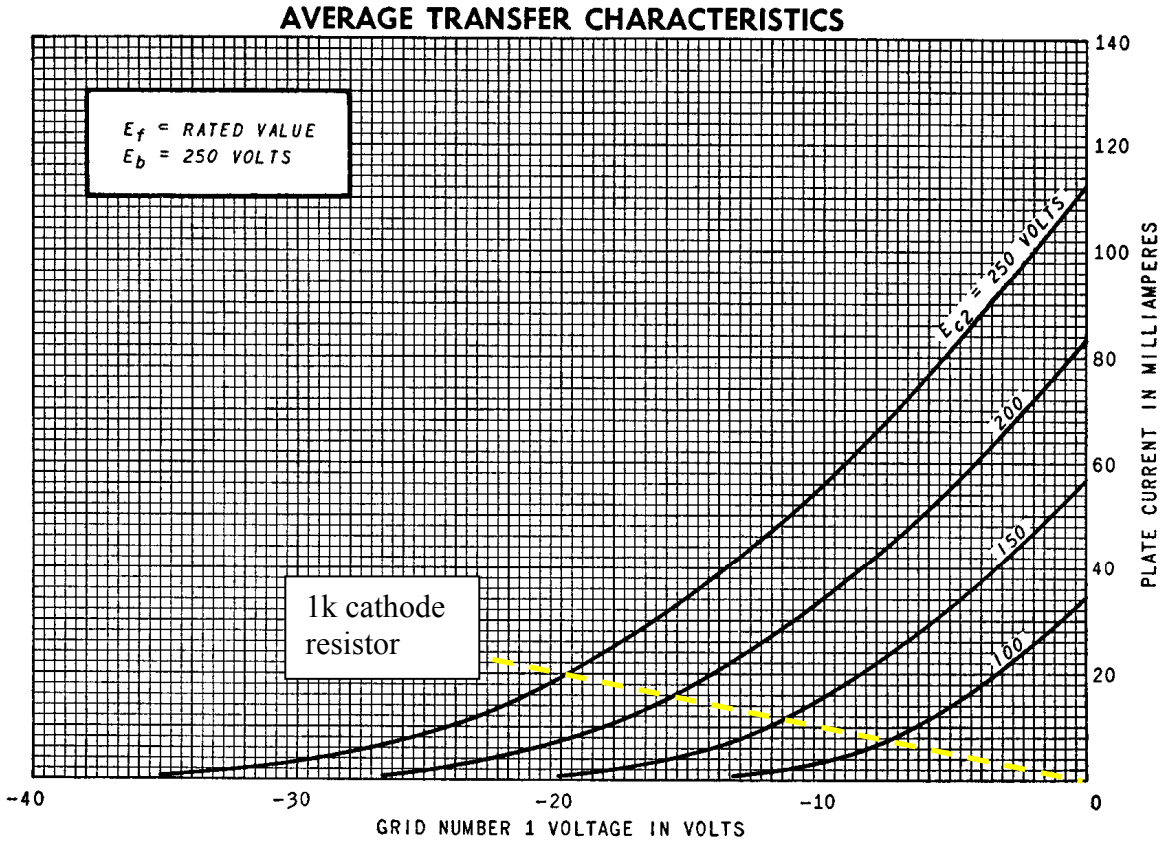
An advantage of VVR over a load attenuator is illustrated in this graphic by the lower power dissipation experienced by the valve.



To illustrate how the loadline can typically stay in the knee region as the anode/screen voltage is reduced by VVR control, the following graph shows the 6AQ5 pentode screen voltage characteristic curves for screen voltages of 100, 150, 200 and 250V. Overlaid on the curves are loadlines for when the anode voltage is also at 100, 150, 200 and 250V, for a constant OPT load. If the loadline generally stays in the knee region as VVR lowers the HT voltage, then the compression type distortion during overdrive should be similar sounding – which is a good outcome!

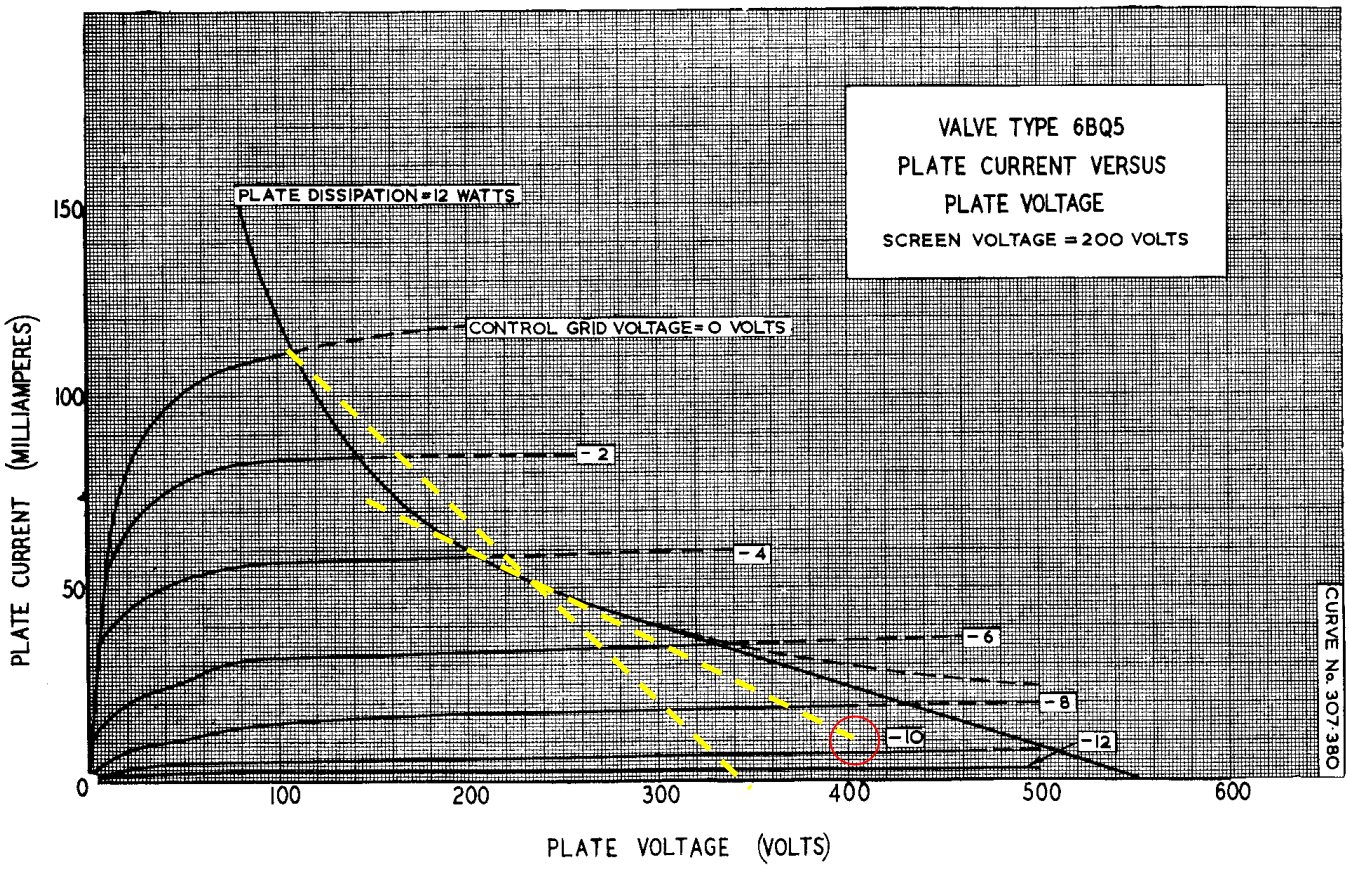


The reduction in idle bias voltage as VVR output voltage reduces is indicated in the following graph for a 6AQ5 valve (although graph is for 250V anode). For a constant cathode resistance (yellow curve = 1kohm), the idle bias voltage reduces from 20V at 250V screen, to under 10V at 100V screen. If the drive level to the output stage can be reduced pro-rata with VVR level, then the symmetry of one grid going to 0V and the other grid going to cut-off appears to be retained. As such, the non-linear transfer characteristic (crowding) around the cut-off region should be little changed (pro-rata) with VVR level, which shouldn't make cut-off distortion any more noticeable.



This change in idle bias voltage means the output drive level from the input stages should ideally be reduced for the same effective overdrive level of the output stage. This level reduction is best done between the PI and the output valves so that the PI stage operates as per normal. For example a pot could replace the grid-leak resistor of the output stage (pot resistance made equal to normal grid-leak resistance so as to retain the same loading on the PI stage). In practise, it may be easier to apply VVR to the PI and output stage, for the reason that a VVR control pot can link in with a master volume pot placed at the input to the PI stage.

An option to consider is to apply the VVR only to the screen supply voltage. Controlling the screen voltage has the main benefit that the power dissipation in the VVR FET is reduced to about 10-20% of the power dissipation needed for normal anode + screen control. In this option, the loadline graphic below shows the situation for an idle voltage are 400V at the anode but only 250V at the screen. Sagging of the HT supply is less as signal levels are lower, so it is assumed the full-load voltage is 350V on anode and 200V on the screen for max signal. Loading impedances don't change. Cathode bias current reduces at idle as screen voltage is 250V. In comparison with the earlier graphics, the loadline is moved significantly away from the general knee zone at peak levels, and into a region where there is little compression as grid voltage reaches 0V. The valve also runs hotter.



VVR protection for over-voltage and over-current

The voltage dropping FET(s) operates with HT level DC voltage, which usually dictates at least a 500V rated FET, and many kits are using higher voltage rated FETs. The capacitive filtering in the power supply rails provides a fairly protected environment from transient over-voltages, especially where the VVR has power supply filter capacitors at both input and output.

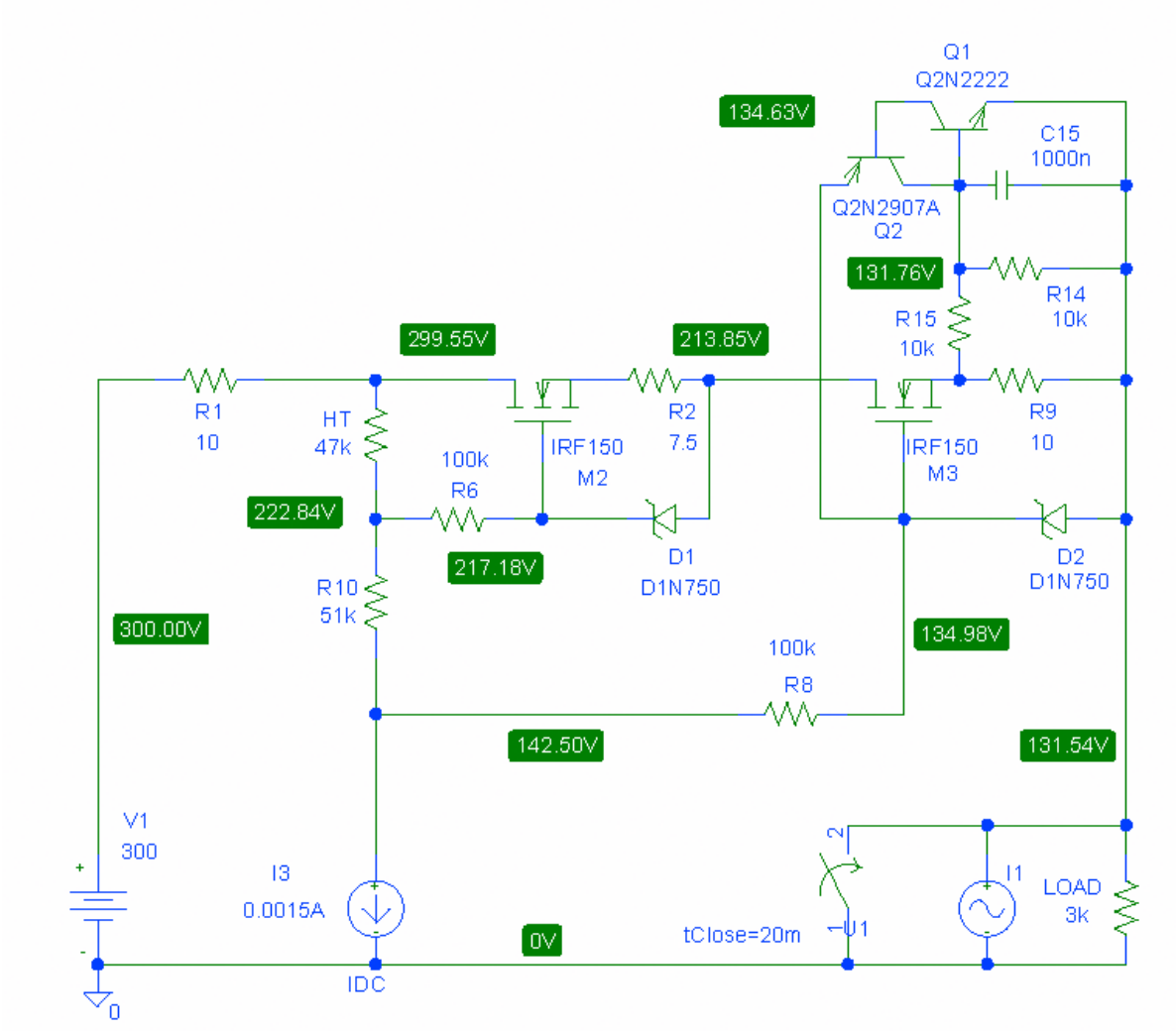
The main voltage dropping FET(s) may experience high levels of transient current and sustained high current under certain circumstances. Worst-case current levels are a short circuit to ground at the output of the VVR, where the HT supply capacitance will initially dump into the short circuit, and then the power supply will continue to source current into the short-circuit. Fusing in the power supply circuit, or fusing related to the shorted path, may take some time to operate. Although the prospective current level may be in the amps, the FET is likely to be rated for the peak current levels capable of being experienced, but the FET is likely to fail from power dissipation levels exceeding the Safe Operating Area and causing excessive junction temperature.

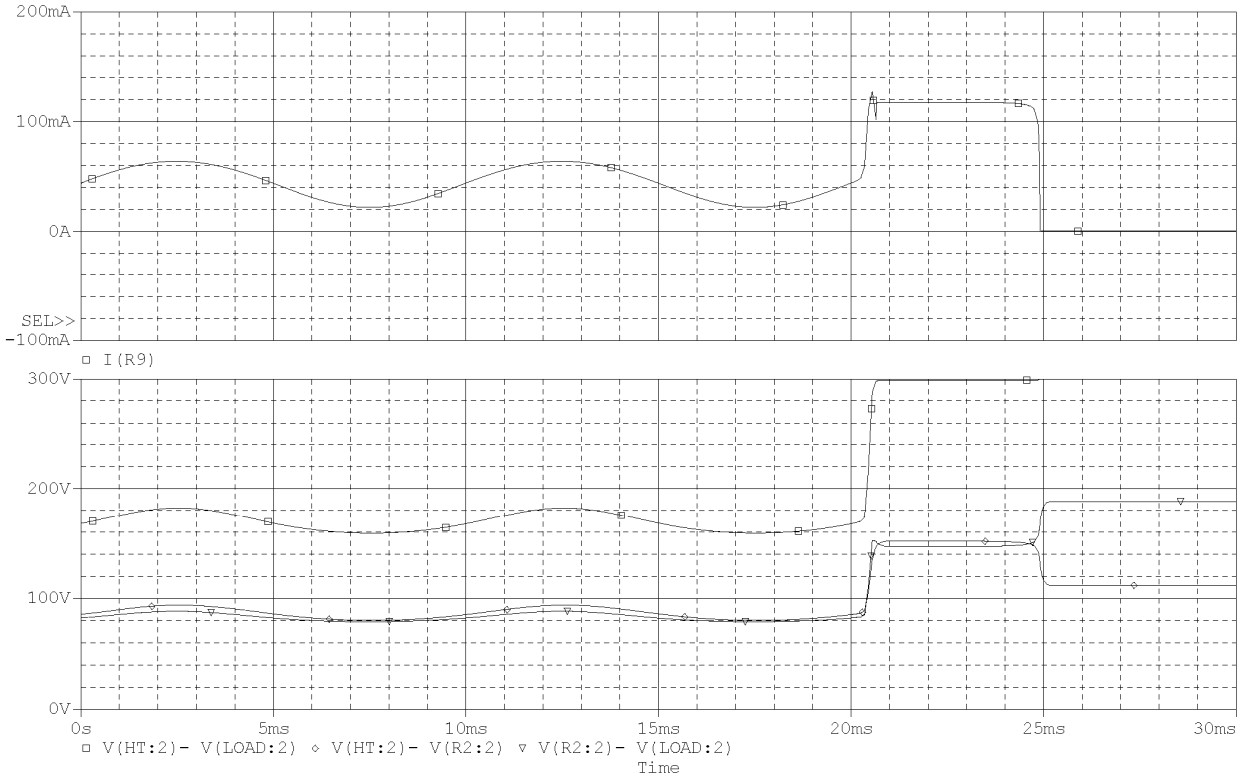
The typical VVR circuit uses a zener diode placed between the main FET's gate and source resistor to provide a simple form of over-current protection. The current limit circuit should be designed so that the FET can normally pass the peak expected current associated with a cranked music level – in which case the VVR would not change the normal sag characteristic under heavy loading when the VVR has a small voltage drop. The peak current levels associated with power-on charging of filter capacitors may be limited somewhat, especially with silicon rectifier diodes, but any delay in charging filter capacitors is likely to be benign compared with normal valve warm-up (less than 1 second for 100mA to charge 100uF to 400V).

The zener diode could be augmented with a foldback circuit to further clamp the main FET current to a lower level if high current levels were sustained due to a short-circuited output – this should be designed to bring the power loss in the main FET down to under the max level experienced by worst-case music. The circuit below shows a two-series FET configuration, with a 4V7 zener diode (D2) to limit short-circuit current to about 120mA. The FET source sense resistor values are adjusted to achieve equal limiting (and hence power dissipation) across each FET.

A foldback clamp circuit is shown using NPN and PNP transistors to bypass the zener diode, with the NPN base turned on through an RC circuit with a short time constant. The thermal resistance of a power FET is less than specified for short durations less than about 100ms, which may complement a short clamp time constant of about 100ms. The trip current limit should be set higher than any peak music demand or power-on capacitor charging demand. The power needs to be turned off and then on to reset the clamp circuit.

The simulation result shows a 40mA nominal loading on the VVR from a 100Hz signal, followed by a short circuited output condition starting at 20ms into the simulation. Initially the short circuit current is limited at 120mA, and each FET drops about the same voltage, but the current level then folds back to 0mA after about 4ms.





FET power dissipation

The junction temperature of the FET(s) must be managed to achieve reliable operation during normal and fault conditions. The heatsink may simply be the amplifier chassis, or a finned radiator heatsink – either way it needs to itself be cooled by external ambient air, and caution exercised if subject to additional heat loading from valves. If the heatsink experiences free ambient air flow then heatsink thermal resistance specifications and normal thermal design calculations can be used for design. If the heatsink is tucked away inside the chassis, or sitting next to an output valve, then thermal design becomes more complicated.

Worst-case FET power dissipation during normal operation is difficult to anticipate, as output stage current levels reduce as VVR voltage drop increases. For the example in Section 0 above, the power dissipation for max sine wave output with 250V idle levels is likely to be 150V VVR drop and a peak VVR current up to 100mA. The FET rms loss is then about 150V x 64mA = 10W. However, cranked waveforms have much higher rms levels, and so power dissipation may be upwards of 12-14W.

Worst-case FET power dissipation during short-circuit load conditions will depend on the over-current protection technique used. For the example in Section 0 above, if a simple current limit of 180mA was provided (as being sufficiently above anticipated peak current levels), and a loaded condition occurred with 250V across the FET, then FET(s) dissipation could be up to 250V x 180mA = 45W. This level of dissipation is way above 12-14W, and so the heatsinking required would be dictated by the over-current protection technique used. Typically, only enough heatsinking would be provided for normal music, and hence FET failure could be expected if any short-circuit type fault occurs.

An example thermal design for an IRFP450 is based on datasheet levels of Rjc=0.65ºC/W, and Rc/hs=1ºC/W, and external conditions of Rhs/amb=5ºC/W, and Tamb=50ºC. For these levels, the maximum steady-state power P that can be dissipated for a 150ºC absolute max junction temperature is then P = (150ºC - 50ºC) / (0.65ºC/W + 1ºC/W + 5ºC/W) = 15W. Note that the

thermal design is primarily limited by the heatsink thermal resistance (Rhs/amb) and the positioning of the heatsink (Tamb).

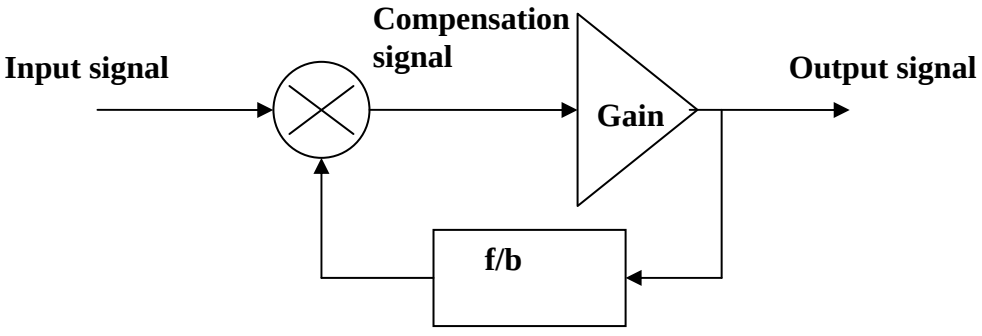
Compromises

Choosing to use VVR can introduce many compromises, and applying a particular VVR implementation to different amps may give different results, which makes VVR performance a very subjective topic. The most obvious compromises relating to VVR include:

- The speaker(s) is not driven hard – this changes the impact of speaker non-linearity.
- The output transformer is not driven hard – this changes the impact of OPT non-linearity.
- The HT supply voltage across the main power supply filter capacitors doesn't sag as much, as the output stage current levels are lower. This may influence both the output stage as well as the PI/pre stages.
- The idle current in a cathode bias output stage will reduce, which may raise the HT supply idle voltage.
- The input stages, if not subject to VVR control, will increasingly overdrive the VVR controlled (output) stage relative to normal conditions, as the VVR stage(s) HT level reduces. This may change the sound character around the overload and cut-off regions.
- The level of feedback, and any presence control if used, will have less effect as the output signal level being fed back is lower.

Feedback

In an amplifier using a feedback loop, say from the speaker output back to the PI stage, then the feedback compensated signal passing through the 'Gain' section will change with VVR control as a result of VVR lowering the gain of the PP output stage. In this example the 'Gain' section includes the PI stage as well as the PP output stage and the OPT. The compensation signal level can be corrected by changing the f/b ratio, so that the compensation signal level remains constant as VVR is lowered. This effect is somewhat equivalent to the influence that a Presence control has on distortion – as the Presence control changes the f/b ratio (but not the Gain) – but be mindful that the Presence control is typically frequency selective by the use of a bypass capacitor.



Practical circuits and references

Some web sites of interest relating to this subject are given below. Practical schematics can be found for the basic circuits. Series connected diodes are typically used to isolate each power supply feed after the main power supply rectifier and filter (ie. a diode for the VVR input, and a diode for the PI and preamp/effects stages). This is to avoid interaction between the VVR and other power supply feeds, and to protect the VVR from reverse current flow. A series diode on

the output of the VVR can also protect the VVR from any reverse current flow from downstream filter capacitors due to any fault condition.

http://www.amptone.com/scholzpowersoak.htm
http://www.motherload.co.uk/
http://www.mavenpeal.com/wattage1.html
http://www.londonpower.com/pscaling.htm
http://hallamplification.com/main.html?src=%2F#2,2
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