Telecom Australia Research Laboratories

770 Blackburn Road, Clayton, Victoria, Australia 3168

Telecommunication Science & Technology Branch

BRANCH PAPER NO.0172

HIGH FREQUENCY, RESONANT DC-DC CONVERSION

BY

T. ROBBINS

Approved by : for General Manager

Approval Date : 24 May 1991

File : Y62/10111.

DISTRIBUTION : GENERAL

FURTHER COPIES : ENQUIRE TELEPHONE NO. (03) 541 6545

HIGH FREQUENCY, RESONANT DC-DC CONVERSION.

Contents

Abstract.

There has been a surge in the availability of compact switch-mode DC-DC converters for 'on-board' distribution of power over the last few years. The power density of these low power (<200W) DC-DC converters has been increased by implementing surface mount and hybrid technology, and by raising the switching frequency. These compact converters are now appearing in Telecom equipment, initially in exchange switching equipment where distributed DC-DC converters are used to power local circuitry from a common 48V DC rail.

To attain the power densities required of on-board converters, the switching frequency within the switchmode power supply has been raised substantially into the hundreds of kilohertz and low megahertz region. Power conversion at these high frequencies is achieved in practice by using resonant circuit techniques. High frequency currents are efficiently switched by employing zero voltage switching resonant techniques, thereby reducing switching losses. The reactive component values required are small, leading to the use of surface-mount ceramic capacitors and multilayer printed circuit inductors/transformers with low profile ferrite cores.

This paper outlines three main circuit techniques for achieving resonant power conversion; quasi-resonant converters, half- and full-bridge multi-resonant converters, and Class E resonant converters. Circuit component performance at the high operating frequencies is assessed.

Experimental investigation of two 48V to 5V DC-DC resonant converters, operating at 1MHz switching frequency with power levels of 50W and 200W, is reported on. The 50W converter uses a single ended Class E resonant topology, and the 200W converter uses a push-pull Class E resonant topology. Simulated and breadboard results are given.

Conclusions are drawn on the development status of resonant techniques, and on component limitations at high frequencies and the potential value of simulation tools in design. The future use within Telecom of compact switchmode power supply equipment for DC-DC converter and rectifier applications is also discussed.

1. INTRODUCTION.

There has been a surge in the availability of compact switch-mode DC-DC converters for 'on-board' distribution of power over the last few years. The power density of these low power (<200W) DC-DC converters has been increased by implementing surface mount and hybrid technology, and by raising the switching frequency. These compact converters are now appearing in Telecom equipment, initially in exchange switching equipment where distributed DC-DC converters are used to power local circuitry from a common 48V DC rail.

Switchmode power supply (SMPS) equipment is also used to convert mains (240VAC) to DC, for instance in plug-packs for portable equipment and in rectifiers for battery charging equipment. The use of high frequency technology in these applications is starting to occur now. For instance, plug-pack power supplies using linear technology have power ratings up to 10W, whereas the use of conventional switchmode technology has increased this to 40W for an equivalent size.

To attain the power densities required of on-board converters, the switching frequency within the smps has been raised substantially into the hundreds of kilohertz and low megahertz region. Power conversion at these high frequencies is achieved in practice by using resonant circuit techniques. The reactive component values required are small, leading to the use of surface mount ceramic capacitors and multilayer printed circuit inductors/transformers with low profile ferrite cores. Ferrite core manufacturers have recently released new material grades to operate efficiently at these higher frequencies.

The efficient switching of high frequency currents can be achieved almost without loss by employing new zero voltage switching (ZVS) resonant techniques. However a trade-off occurs in using ZVS, due to the voltage (V) and current (I) stress on the switching device. In Figure 1.a) the V and I waveforms are shown for a **square-wave type** converter over one switching period. At the switching transitions there exist overlaps of V and I across the device, causing a (switching) power loss that is frequency dependant. This switching loss characteristic is the main reason for the trend to move away from square-wave converters to ZVS resonant converters at high frequencies. In Figure 1.b) the V and I waveforms are shown for a **ZVS resonant type** converter, where there is no overlap of V and I at the switching transitions, but there are higher levels of V and I on the device during the period. The advantage of using ZVS resonant topologies can outweigh the need for a higher V-I rated power Mosfet switch in low voltage applications. Using ZVS for 240V AC applications requires a high voltage switch technology, such as IGBT's, with a subsequent reduction in high frequency capability.

A variety of resonant circuit topologies that operate with ZVS are being researched worldwide, and a small number of

commercial DC-DC converters are now available. One strong research group is the Virginia Power Electronics Center (VPEC) at the Virginia Polytechnic Institute and State University, USA, with research on half- and full-bridge ZVS multi-resonant converters [1] as well as running frequent courses to industry on resonant converters. Another ZVS topology called Class E [2] has been analysed in detail [3,4], but little experimental work has been reported on Class E DC-DC converters [5]. Simulation software such as the general circuit analysis program PSpice are useful tools for converter designers, and there is specially developed software (RESOCAD II) [6] available for the design of Class E converters.

The state of research in ZVS circuit topologies is still in its infancy, with attention being paid to reducing the switch V-I stress under all operating conditions. An ideal scenario would be to couple the waveform shape of a square-wave converter with the ZVS transitions of a resonant converter. This outcome has been achieved under limited operating conditions by Statronics Power Supplies [7].

DC-DC converters are in widespread use in Telecom exchanges, both in AXE switching equipment and in ancillary equipment designed in-house. Square-wave topologies are presently used in these converters. Future applications in Telecom for high power density SMPS may be in powering fibre to the kerb/home equipment, and in distributed powering of the exchange 48V DC rail using lower power rectifiers (200-300W)[8] rather than the present 500W to 10kW switchmode rectifiers.

Section 2 outlines three main circuit techniques for achieving resonant power conversion; quasi-resonant converters, half- and full-bridge multi-resonant converters, and Class E resonant converters. Circuit component performance at the high operating frequencies is assessed in Section 3.

Experimental investigation of two 48V to 5V DC-DC resonant converters, operating at 1MHz switching frequency with power levels of 50W and 200W, is reported on in Section 4. The 50W converter uses a single ended Class E resonant topology, and the 200W converter uses a push-pull Class E resonant topology. Simulated and breadboard results are given.

Conclusions are drawn in Section 5 on the development status of resonant techniques, and on component limitations at high frequencies and the potential value of simulation tools in design. The future use within Telecom of compact switchmode power supply equipment for DC-DC converter and rectifier applications is also discussed.

2. RESONANT POWER CONVERSION.

Switchmode DC-DC converters provide power conversion from one DC level to another, utilising a semiconductor switch(es) operating only in the on and off states (not in linear mode). The input DC source is converted into AC by the switch(es) and associated reactive components (capacitors, inductors-transformers), and then the AC is rectified and filtered to give a DC output. By control of the switching operation and/or using a transformer the conversion achieves DC to DC transformation at a controllable ratio.

Resonant power conversion is achieved when sinusoidal AC voltages and/or currents are generated to transfer power from the input to output. The major advantage in using resonant conversion is that the switch can be allowed to turn on and/or off with zero voltage and/or zero current across the device, thereby reducing switching loss. To achieve either zero voltage switching (ZVS) and/or zero current switching (ZCS), the switch is embedded in a circuit with reactive components that shape the voltage/current waveforms generated across the switch. Different circuit topologies achieve a varying degree of success in providing ZVS/ZCS with minimal circuit and switch control complexity. In general, ZVS offers more advantages when practically implemented than ZCS.

A number of benefits arise from using resonant conversion, compared with square-wave conversion:

- lower switching losses allow a higher operating frequency to be used, with subsequent reduction in converter size and weight.
- smooth voltage and current waveforms combine with ZVS/ZCS to reduce the generated noise (EMI) at frequencies above the fundamental switching frequency.
- circuit and component parasitic elements are generally included in the circuit topology.
- converter transient response improves relative to the switching frequency.

The main trade-off existing between resonant and square-wave conversion is the higher voltage and current stress levels generated in the resonant circuit. Put simply; a square AC waveform has a lower peak value for a given rms level than a sinusoidal waveform.

Three circuit techniques for achieving resonant power conversion are described in the following subsections; quasi-resonant converters, half- and full-bridge multi-resonant converters, and Class E resonant converters. A collection of 41 papers [1] provides a comprehensive overview of the various classes of resonant converters.

2.1 Quasi-Resonant Converters.

In quasi-resonant converters (QRCs) the switch waveforms are

modified by the addition of reactive circuit components used to achieve ZVS or ZCS. Many quasi-resonant topology combinations can be made by inserting simple series inductor /parallel capacitor networks into square-wave topologies.

The basic down converter, or buck converter, topology is shown in Figure 2 with two quasi-resonant circuit configurations. Figure 2.a) has the resonant capacitor C_R placed across the switch, along with a resonant inductor L_R in series, to provide ZVS. Figure 2.b) has the resonant capacitor placed across the diode to provide ZCS.

In the ZVS down converter the off-state switch voltage waveform (equal to V_{CR}) rises slowly from zero, resonates to a peak voltage of twice V_{IN} and returns slowly to zero before the switch is turned on, achieving ZVS. A similar switch current waveform occurs in the ZCS down converter. However the practical performance of these QRCs is severely degraded, by parasitic circuit elements such as the switch and diode internal capacitances, and by input voltage and output current regulation.

In summary, QRCs generate half-sinusoid pulses of voltage or current in the switch circuit and integrate some of the major parasitic circuit elements into the circuits operation, thereby achieving marginally better high frequency performance compared to square-wave converters.

2.2 Half- and Full-bridge Multi-resonant Converters.

Multi-resonant conversion (MRC) is an extension of QRC, that integrates all the major parasitic circuit elements to allow ZVS/ZCS of both the switch(es) and diode rectifier(s). This allows MRCs to operate at higher switching frequencies than QRCs.

Single-ended (one switch) QRC and MRC topologies operating with ZVS have a major disadvantage of high voltage stress on the switch, typically several times the input voltage. For 240V AC applications the rectified DC voltage of 340V means switch voltage ratings over 1kV, ruling out the use of high speed power Mosfets. Lower voltage stress levels are produced in multiple switch topologies, such as push-pull, half-bridge (HB) and full-bridge (FB), due to the automatic clamping action of the conducting switch on the complementary switch off-state voltage.

A FB-ZVS-MRC is shown in Figure 3. The resonant capacitors C_1 - C_4 in parallel with the switches Q_1-Q_4 incorporate the output capacitances of the Mosfet switches, (and D_1-D_4 represent their body diodes). The series resonant inductor L incorporates the transformer leakage inductance. The rectifier diode resonant capacitors C_{DR1-2} incorporate the diode junction capacitances. Regulation over the full load range is achieved with wide-band frequency control (typically 5:1 ratio between minimum and maximum operating frequency).

The main disadvantage with the FB- and HB-ZVS-MRC is the wide-band frequency control required for regulation. This characteristic causes a number of practical design constraints:

- Component losses are highest at f_{MAX} (full load)
- Filter component values are designed for f_{MIN}
- Transient response is determined by f_{MIN}.

In summary, the HB- and FB-ZVS-MRC are preferred for high input voltage applications where the voltage stress is limited to the input voltage level. High frequency operation is achievable, but not all the power density advantages are realised due to the wide-band frequency control requirements.

2.3 Class E Resonant Converters.

Class E resonant converters provide regulated DC-DC conversion over a wide load range using only narrow-band frequency control. This is achieved by incorporating a series resonant LCR tank network, of moderate Q, in a ZVS/ZCS topology.

Both single-ended and push-pull ZVS topologies are shown in Figure 4. The push-pull topology does not provide any voltage stress limiting, compared to the HB- and FB-ZVS-MRC, however its symmetry does suppress even-order harmonics in the primary current thereby achieving improved rectifier performance.

In the single-ended ZVS topology, the inductor L1 acts as an input current source and a half-sinusoid voltage waveform is generated across the switch due to the shunt capacitance C1 and the series resonant tank, L2-C2-transformer load. The switch current waveform is nearly a half-sinusoid, rising from zero and then just after reaching a maximum, the current falls to zero as the switch turns off. The switch ideally exhibits ZVS at both turn-on and turn-off, as well as ZCS at turn-on, however ZVS is lost at turn-on under certain operating conditions. Mosfet output capacitance is incorporated into C1, and transformer leakage inductance is incorporated into L2.

Multi-resonant Class E converters have recently been introduced [9], but as yet only single diode rectifier circuits have been analysed.

In summary, Class E resonant converters achieve narrow-band frequency control, along with high frequency operation and comparable voltage and current stress levels to other single-ended resonant converters.

2.4 Further Considerations.

The state of research in ZVS/ZCS circuit topologies is still in its infancy, with most attention being paid to:

- Using pulse width modulation (PWM) control to replace wide-

band frequency control.
- Reducing the switch V-I stress under all operating conditions.
- Achieving ZVS/ZCS under all operating conditions.

For example in the Class E resonant converter, ZVS is lost at turn-on under certain operating conditions. Methods to alleviate this characteristic include duty-cycle control in conjunction with frequency control [10], and switch-controlled inductors and capacitors to re-tune the resonant tank network [11].

An ideal scenario for high frequency power conversion would be to couple the waveform shape of a square-wave converter with the ZVS/ZCS transitions of a resonant converter. This outcome has been achieved under limited operating conditions by Statronics Power Supplies [7].

The experimental investigation of two Class E resonant converters is reported on in Section 4.

band frequency control.
- Reducing the switch V-I stress under all operating conditions.
- Achieving ZVS/ZCS under all operating conditions.

For example in the Class E resonant converter, ZVS is lost at turn-on under certain operating conditions. Methods to alleviate this characteristic include duty-cycle control in conjunction with frequency control [10], and switch-controlled inductors and capacitors to re-tune the resonant tank network [11].

An ideal scenario for high frequency power conversion would be to couple the waveform shape of a square-wave converter with the ZVS/ZCS transitions of a resonant converter. This outcome has been achieved under limited operating conditions by Statronics Power Supplies [7].

The experimental investigation of two Class E resonant converters is reported on in Section 4.

3. HIGH FREQUENCY COMPONENT TECHNOLOGY.

The performance of circuit components degrades with increasing frequency, due mainly to component parasitic elements and frequency dependent power losses. Converter power density initially increases with increasing frequency due to smaller passive component values, but then the power density reduces as frequency dependent power losses become significant. The maximum power density achieved is a function of component performance and allowable temperature rise (reliability) of the component. Passive and active component performance at high operating frequencies is assessed in this Section.

3.1 Capacitors.

The type of capacitor used in high frequency power conversion is largely determined by parasitic inductance (equivalent series inductance - ESL) and parasitic resistance (equivalent series resistance - ESR). Fortunately, the requirement for small values negates the need for electrolytic types, and their inherent low reliability. Suitable capacitor types have ceramic, silvered-mica and porcelain dielectrics, and are used extensively in RF applications. Generally, ESL is minimised by small package dimensions and by incorporating ESL into the circuit network. ESR becomes important when large resonant currents exist and low ESR capacitors such as silvered-mica and porcelain types should be used. For filter applications, multiple ceramic surface mount capacitors with low voltage ratings provide good performance.

3.2 Inductors/Transformers.

Inductor design is complex, due mainly to the following factors:

- The component is relatively large, having a significant affect on the achievable power density.
- Power losses are distributed between the core and winding, and are characterised by many variables, in particular the winding geometry.
- The preferred winding construction is changing from conventional litz/foil/single wire coils to an integrated multi-layer printed circuit winding.
- Stray magnetic fields can couple with other circuitry.
- Cores are available in a wide variety of materials, shapes and sizes.
- Only a few inductor/transformer design software packages are available, and none take into account all high frequency characteristics.

Ferrite core inductors/transformers are the preferred type, compared with air cored, due to the low external magnetic field. The ferrite core has two main operating constraints - flux saturation and power loss. The magnetic flux density B is given by:

$$B = L.I.10^3/(N.Ae) \quad ,(mT) \quad (1)$$

where,

L = inductance (uH)
I = current, rms (A)
N = turns
Ae = effective core area (mm^2)

At low operating frequencies the core saturation limit of approximately 300-500mT determines the minimum core size. At high operating frequencies the core power loss limits the flux density level to below the saturation limit. For a core volume VCORE, the core power loss PCORE is given as,

$$PCORE \propto VCORE \times B^{2.4} \times f^{1.6} \qquad (2)$$

State-of-the-art core loss is around $4W/cm^3$ @100mT @1MHz @80°C.

In general the core size reduces in inverse relation to the operating frequency, with only a flux saturation limit imposed. When the frequency is high enough to impose power loss limits then no substantial improvement in power density is achieved with increased frequency. Criticism of converters operating well into the MHz range (8MHz [11], 22MHz [12]) has been reported in [13]. In these reports the ferrite cores are being operated at very low flux levels (<10mT) highlighting the low power density achieved.

Coil winding techniques change dramatically as frequencies exceed 50-100kHz. Skin depth is inversely proportional to the square root of frequency and at 300kHz is about 0.1mm. To achieve effective high current carrying capacity at high frequencies round wire is replaced by litz/foil windings. Multi-layer printed circuit windings, where 1oz. copper layer thickness is 0.035mm, integrate well with surface-mount construction and have good high frequency performance.

A good example of surface-mount multi-layer PCB construction is the 8 layer PCB transformer with a centre-tapped secondary connected to surface mount diode die made by Statronics [15], shown in Figure 5, that is used in the 50W converter operating at 1MHz described in Section 4. Core loss in this transformer is minimised by reducing the centre and outer leg lengths of the core to a minimum. A design trade-off can be made with the width of the centre core leg (leg cross section area) and the winding window width. In Figure 5 the centre leg width is reduced by about 50% from nominal, giving more winding room and hence lower winding loss. Core loss in the leg marginally increases due to a higher flux density in a smaller core volume.

3.3 Active Devices.

Schottky barrier diodes have a substantially lower on-voltage and exhibit no reverse recovery phenomena compared with pn junction diodes, which both improve on rectifier efficiency especially for low output voltages of 5V to 12V. However the large junction capacitance of Schottky diodes, which is

voltage dependent, becomes a major parasitic circuit element at high frequencies. Ideally the junction capacitance should be incorporated into the circuit's operation, as in MRCs, or it will seriously degrade rectifier performance. Diode operation in MRCs is subject to voltage stress levels up to four times the output voltage, requiring a 250V device for 48V output conversion. Recently schottky diodes with voltage ratings up to 150V have become available, with the expectation of at least 200V devices soon.

Power Mosfets have proven themselves to be the fastest, most practical and reliable switching device with voltage ratings up to 600-1000V. Performance has improved steadily since market entry in the mid '70s by reducing gate and drain-to-source (on) resistance and terminal capacitances, as well as increasing reliability and ruggedness to dv/dt, di/dt and overvoltage transients. The Mosfet structure can be integrated with standard MOS and bipolar processing to give Smart IC devices. Mosfet models for circuit simulation [16] give accurate waveform detail and transition times at operating frequencies up to 5-10MHz.

Specialised gate driver ICs for power Mosfets have recently been developed to interface TTL low level signals with the high current pulse requirements (2-10A) of Mosfet gates operating efficiently at high frequencies. In the past designers have had to build discrete drive circuits to achieve fast switching times. Dual driver ICs are available in one package with inverting, non-inverting and complementary outputs for push-pull and bridge topologies, as well as isolated outputs for 'high side' switches such as in buck and bridge topologies.

Control circuit ICs have been developed for many of the square-wave and some of the resonant topologies with maximum operating frequencies of 1-2MHz. So far no control circuit has been developed to implement a variable frequency - constant duty cycle characteristic for use with Class E resonant converters.

Variable f / Variable D → see APEC'90 p122-3

4. EXPERIMENTAL INVESTIGATION OF CLASS E RESONANT CONVERTERS.

Experimental investigation of two 48V to 5V DC-DC resonant converters, operating at 1MHz switching frequency with power levels of 50W and 200W, is reported on in this section. The 50W converter uses a single-ended Class E resonant topology as shown in Figure 4.a), and the 200W converter uses a push-pull Class E resonant topology as shown in Figure 4.b). Simulated and breadboard results are given on both converters.

Single-ended Converter.

Figure 6.a) shows a circuit of the single-ended Class E resonant converter incorporating a Class E inverter with C_2-L_2 tank, followed by a transformer matching network with centre-tapped secondary, full-wave rectifier and capacitively filtered output. Analysis for the Class E inverter is well reported [3]. Kazimierczuk and Bui [4] provide an analysis of the transformer/rectifier/load and design equations for the converter, which are summarised below.

The analysis assumes that all components are ideal, L_1 is large (effective current source) and that the loaded Q factor of the C_2-L_2 tank is large ($Q \geq 5$) so that the current i is a sine wave (no harmonics) where $i = I_m \cos\omega t$. The transformer/ rectifier circuit can be replaced by a square-wave voltage source as shown in Figure 6.b), by neglecting the voltage drop across the rectifier diode D2 and D3, where $v = \pm nV_o$. The inductor L_3 (transformer self or magnetising inductance) acts as both a matching network between the C_2-L_2 tank and the rectifier load, and as an inductive impedance inverter [17]. The current through L_3, i_{L3}, is a symmetrical triangle wave where $v = X_{L3} \cdot \partial i_{L3}/\partial(\omega t)$ and $X_{L3} = \omega . L_3$.

The input current of the transformer is $i_R = i - i_{L3}$, giving current i_D at the input to the load network C_f-R_L as $i_D = n|i_R|$, and hence the DC load current is,

$$I_o = (1/\pi) \int i_D \, \partial(\omega t) = 2n . I_m . \cos\phi/\pi \qquad (3)$$

where ϕ is the phase of the fundamental component of v.

Lossless operation of the Class E inverter can be obtained for $0 \leq R \leq R_{max}$ in Figure 6.d), whereas converter load resistance R_L is usually in the range $R_{Lmin} \leq R_L \leq \infty$. This impedance incompatibility can be removed by using a matched load network C_1-C_2-L_2-L_1, as in Figure 6.c) in which impedance inversion can be achieved [17].

An experimental Class E converter has been designed to operate at a nominal switching frequency of 1MHz. For a 50W output at V_o=5V, the minimum load resistance is R_{Lmin}=0.5Ω. The schottky diodes D2 and D3 have a forward voltage drop V_F=0.4V giving a rectifier efficiency $\eta_R = 1/(1 + V_F/V_o) = 92.6\%$. Assuming the Class E inverter efficiency is η_E=95% and the transformer efficiency is η_T=95% then the total converter efficiency is η =

$\eta_E.\eta_T.\eta_R$ = 83.6%. The DC input power is $P_{iMAX} = P_{oMAX}/\eta$ = 59.8W and the input current at V_i=48V is I_{iMAX}=1.25A. From [4] the converter component design equations are, where V_i=48, $\omega=2\pi f$, and f=1MHz;

$$R_{MAX} = 0.5249\ V_i^2 / P_{iMAX} = 20.2\Omega$$

$$C_1 = 0.2067 / \omega.R_{MAX} = 1.63nF$$

$$C_2 = 0.2269 / \omega.R_{MAX} = 1.79nF$$

$$L_2 = 4.673\ R_{MAX} / \omega = 15.0\mu H$$

$$L_3 = \pi.R_{MAX} / 8.f = 7.9\mu H$$

$$n = (\pi/2)\sqrt{(R_{MAX}/R_{LMIN})} = 10 \text{ turns}$$

Component stresses are;

$$V_{SMAX} = 3.61V_i = 173V$$
$$I_{SMAX} = 2.78I_{iMAX} = 3.5A$$
$$I_{DMAX} = 1.67I_{oMAX} = 16.7A$$
$$V_{DRMAX} = -2V_o = -20V$$
$$V_{C2} = X_{C2}.I_m = \pi I_{oMAX}/(2n.\cos\phi.\omega C_2) = 198V$$

where these values decrease with load.

After the design stage the circuit was simulated using PSpice, with the component values calculated above and accurate high frequency models of a 200V Mosfet (IRF640) and a low on-voltage schottky diode. The PSpice circuit listing is given in Appendix A. Resistive component losses were lumped into a tank series resistance RL2 and two secondary winding resistances RLS1 and RLS2. The transformer core was modelled for a PQ 2020 size core and the gap was adjusted to give the required magnetizing inductance L_3.

Correct circuit operation was obtained with a slight change to the component design value for C_1, due to the non-linear contribution from the Mosfet output capacitance. With the correct value of C_1, ZVS was achieved at both switching transitions and ZCS at turn-on, as shown in Figure 7. The simulation results correlated well with the circuit analysis [4], except for an asymmetry in the rectifying diode currents caused by harmonics in the primary current. The analysis [4] assumes a sinusoidal primary current composed only of the fundamental, whereas the simulation results show the correct harmonic structure obtained from the Class E inverter [18]. The dominant second harmonic causes an asymmetric current flow between the centre-taped secondaries, resulting in a diode current imbalance of the order of 1.5:1 as shown in Figure 8. This imbalance may be alleviated by a number of methods; increasing the inverter tank Q, changing the turns ratio between the secondary halves, or using a single-ended rectifier; all of which have significant shortcomings.

A breadboard converter was constructed using low loss components achieving 87% efficiency at 5V, 50W output. This level of efficiency is high compared with typical levels of about 75%-85%. A custom designed 8 layer PCB transformer and surface mount rectifier/filter from Statronics [15] were used in the construction.

The inductor L_2 was made using custom PCB windings. The annular windings, of 1, 2 or 3 turns per side on a double-sided PCB, were sized to fit PQ2020 cores and were effective in breadboarding both inductors and transformers. To reduce the loss in inductor L_2, a series connection of three 5μH inductors were used. Each 5μH inductor comprised 9 turns (made from 5 PCB windings) placed in half a PQ2020 core set of Magnetics K material with an air gap resulting from the open end of the core. This arrangement of three series inductors reduced the total inductor loss by operating each core at a lower flux density, resulting in a significant reduction in core loss.

Observable circuit waveforms correlated well with the simulation results. Component values were optimised to give ZVS on the Mosfet, with C_1=1.33nF and C_2=1.94nF being within 10% of the simulated and design estimates. The switch current waveform, and hence ZCS, could not be observed due to the short lead lengths and PCB surface-mount construction. Accommodating a current probe in the circuit would severely degrade operation due to induced voltages from the $L\partial i/\partial t$ of the extra lead length. The asymmetric rectifier currents could not be observed directly for the same reasons as the switch current.

An indirect method of observing asymmetric rectifier currents is to examine the filter capacitance voltage waveshape. The capacitor waveshape will be a distorted sinusoid due to the asymmetric current pulses flowing from the rectifier diodes. Figure 9 shows the good correlation between the simulated and measured capacitor voltage waveforms.

Load regulation is achieved by narrow-band frequency control, however ZVS at turn-on is lost as the resistance increases from R_{LMIN}. ZVS at turn-on can be regained by varying the duty-cycle in conjunction with the frequency. Figure 10 shows the converter switch voltage at 5V, 2.5W output with a) frequency control only and b) frequency and duty-cycle control. Note the reduced input power needed for b).

Converter efficiency with 50W output was 87% with the 7.1W loss dominated by the output diodes, inductor L_3 and transformer. The diodes have a measured on-voltage of 0.4V, resulting in a 2.5W loss in diode D1 and 1.5W loss in diode D2, due to current asymmetry. The other circuit losses could not be quantified, however the finger temperature test indicated that inductor L_3 and the transformer were the only other significant loss components.

Push-pull Converter.

The design for the push-pull Class E converter of Figure 4.b) varies slightly from that of the single ended converter. The push-pull topology doubles the voltage excursion across the transformer primary and doubles the primary current, thereby quadrupling the output power.

The single-ended converter design equations can be used for the push-pull design by noting that each half of the push-pull circuit operates essentially in isolation to the other half, except that each half now has double the input power for the same input voltage. For a 200W output power and 5V output the output resistance R_{Lmin} is a quarter of the 50W design. The push-pull circuit values are then $R_{MAX}=10.1\Omega$, $C_1=3.26nF$, $C_2=3.6nF$, $L_2=7.5\mu H$, $L_3=4\mu H$, n=14.

The circuit was then simulated and a breadboard converter circuit was constructed using low-loss components. However full output power could not be achieved due to excessive temperature rise in the magnetic cores of the inductor L_2 and the transformer, resulting from the high operating flux densities. Lower flux density can be achieved by increasing the relative core size (Ae in equation 1), however this was not an available option. Instead the operating frequency was halved to 500kHz, reducing core loss by 80% (equation 2).

The circuit was simulated and the listing is given in Appendix B. Correct circuit operation was obtained with a slight change to the component design value for C_1, due to the non-linear contribution from the Mosfet output capacitance. With the correct value of C_1, ZVS was achieved at both switching transitions and ZCS at turn-on, as shown in Figure 11. The simulation results show no sign of any asymmetry in the rectifying diode currents, and a fourier analysis of the primary current showed a negligible level of even order harmonics. The breadboard circuit was reconfigured with C1, C2, L2 and L3 doubled.

To construct the transformer a 12 turn primary was interleaved around the 2 turn secondary on a PQ2020 core with the double-sided PCB windings. Interleaving the primary and secondary windings reduces the interwinding field strengths, and hence the frequency dependent losses [19]. The primary was constructed from 12 turns, and not 14, to reduce the number of primary PCB winding layers to 2, each with 6 turns (3 turns per side).

Converter efficiency with 5V, 200W output at 40V input was 77% operating at 510kHz. Forced air cooling of the transformer was needed for full load operation. The Mosfet drain-source voltage and output voltage ripple waveforms at full load are shown in Figure 12. The sinusoidal output voltage ripple is free of transients, and shows a slight asymmetry due most likely to even-order harmonics in the primary.

Circuit simulation using a commercial SPICE software (PSpice) was an effective tool during both the initial design verification stage, and for further investigation of circuit asymmetry which was not apparent from the design literature. In a complete design scenario (manufacturing), the software is capable of performing other important tasks, such as tedious parameter variation and stability analyses. The processing speed was adequate, with a 386 machine running a co-processor at 33MHz completing a transient analysis from power-on to steady state (~20 to 40 cycles) for 2 separate push-pull circuits (for comparison purposes) in 7-10 minutes. Figure 13 shows the simulated output voltage of a push-pull converter during the first 25 cycles after power-on.

5. CONCLUSIONS.

Increased power density can be achieved in switchmode DC-DC converters by increasing their switching frequency. Operation at higher switching frequencies involves the use and application of both advanced components and techniques such as zero voltage switching (ZVS) in resonant circuits. The design process is non-trivial and many trade-offs are needed to achieve a balance between reducing component size and increasing circuit losses that are frequency dependent.

ZVS operation at high switching frequencies can be achieved through resonant power conversion. Three circuit techniques applying resonant power conversion have been outlined; quasi-resonant converters, half- and full-bridge multi-resonant converters, and Class E resonant converters. The various disadvantages associated with each converter topology are presently receiving worldwide research input. Significant performance improvements appear likely in the next few years, making comparisons between topologies an untimely exercise.

Two Class E 48V-5V DC-DC resonant converters have been simulated and breadboarded; a 50W single-ended converter and a 200W push-pull converter. Magnetic components were clearly shown to be the limiting component in converter performance and power density. Trade-offs made in the design of the two breadboard converters resulted in maximum practical switching frequencies of 500kHz to 1MHz. Above this frequency range core losses become excessive and the core power handling density reduces. Most other circuit components are capable of operating at higher frequencies, although the controller ICs presently operate at frequencies below 1 or 2MHz.

Circuit simulation using a commercial SPICE software (PSpice) was an effective tool during both the initial design verification stage, and for further investigation of circuit asymmetry which was not apparent from the design literature.

DC-DC converters are in widespread use in Telecom exchanges, both in AXE switching equipment and in ancillary equipment designed in-house. Square-wave topologies are presently used in these converters. Telecom has no direct control of what power supply technology is used in the AXE switching equipment. Various in-house equipment projects have/are considering the use of on-board DC-DC converters instead of discrete designs.

Telecom has a major requirement for 240V/415VAC-48VDC rectifiers in the power range from 600W to 10kW. Switchmode rectifiers (SMRs) presently use two power conversion stages to convert the 240VAC, firstly to 400VDC, and then by a second stage to 48VDC. The majority of manufacturers use square-wave power conversion techniques for both stages due to the high operating voltages at the input of both stages. The use of square-wave conversion has kept switching frequencies below 100kHz, limiting further improvements in power density. One

manufacturer, Eltec, uses resonant conversion in the second 400VDC-48VDC stage operating at a switching frequency of 200kHz. The SMR power conversion techniques used in this power range are not expected to change markedly in the near future.

The future use of lower power SMRs (<500W) within Telecom is likely in two major areas. The first area may be in a compact modular distributed power system for exchanges, presently being assessed by F.Bodi, Telecommunications Power Section, Telecom Network Engineering, with a prototype system being developed by Power Reflex under a Product Development Fund grant. The SMR power rating used in this prototype system is 300W. The second area may be in powering optical fibre equipment in the CAN using battery storage, with the SMR positioned either at the kerb or in the customer premises. The SMR power range for this application is expected to be between 5-100W.

Low-power SMRs for telecommunications use have not yet been fully developed, and it is in this area that the use of high frequency ZVS topologies using resonant conversion appear certain to make a significant impact.

Acknowledgements.

The author would like to thank Rod Tuson, Statronics Power Supplies, Hornsby N.S.W., for contributing componentry, and Graeme Brownfield for testing potential control circuits.

References.

[1] "High-frequency resonant, quasi-resonant, and multi-resonant converters", Virginia Power Electronics Center, Volume 1.

[2] N.O.Sokal & A.D.Sokal, "Class E, a new class of high-efficiency tuned single-ended switching power amplifiers", IEEE J.Solid-State Circuits, Vol.SC-10, No.3, June 1975, pp.168-176.

[3] M.K.Kazimierczuk & K.Puczko, "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle", IEEE Trans. Circuits & Systems, Vol.CAS-34, No.2, Feb.1987,pp.149-159.

[4] M.K.Kazimierczuk & X.T.Bui, "Class E dc/dc converters with an inductive impedance inverter", IEEE Trans.Power Electronics, Vol.4, No.1, Jan.1989, pp.124-135.

[5] R.Redl & N.O.Sokal, "High-frequency switching-mode power converters: general considerations, and design examples at 0.6, 1, and 14 MHz", Proc. High Frequency Power Conversion 1986 Conference, pp.265-296.

[6] N.O.Sokal & R.Redl, "Computer program for fast simulation and optimisation of single-ended inductor-fed zero-voltage-switching series-resonant dc/dc converters and dc/ac inverters with any loading topology", IEEE Proc. Applied Power Electronics Conference 1989.

[7] R.Tuson & I.Dimanstein, International Patent Application PI5168 (Australia) "High efficiency converter".
[8] F.Bodi, "Distributed power systems", International Telecommunications Energy Conference 1988, pp.143-150.
[9] M.K.Kazimierczuk & J.Jozwik, "Resonant dc/dc converter with class-E inverter and class-E rectifier", IEEE Trans. on Industrial Electronics, Vol.36, No.4, Nov.1989, pp.568-578.
[10] R.Redl & B.Molnar, "Design of a 1.5MHz regulated dc/dc power converter", Proc. PCI/MOTOR-CON, Sept.1983, pp.74-87.
[11] W.Gu & K.Harada, "A new method to regulate resonant converters", IEEE Trans. on Power Electronics, Vol.3, No.4, Oct.1988, pp.430-439.
[12] M.M.Jovanovic, W.A.Tabisz & F.C.Lee, "Zero-voltage switching technique in high-frequency off-line converters", IEEE Proc. Applied Power Electronics Conference 1988, pp.23-32.
[13] W.C.Bowman et al., "A resonant dc-to-dc converter operating at 22 megahertz", IEEE Proc. Applied Power Eleçtronics Conference 1988, pp.3-11.
[14] S.Cuk, Z.Zhang & L.A.Kajouke, "Low profile, 50W/in^3, 500kHz integrated-magnetics PWM Cuk converter", Proc. High Frequency Power Conversion 1988 Conference, pp.442-463.
[15] Courtesy of Rod Tuson, Statronics Power Supplies, Hornsby, NSW.
[16] T.P.Robbins, "Electromagnetic interference prediction of a flyback switchmode power supply using simulation techniques", Proc. International Telecommunications Energy Conference 1989, pp. 16.2/1-7.
[17] M.K.Kazimierczuk & K.Puczko, "Impedance inverter for class E dc\dc resonant converter", Midwest Symposium on Circuits and Systems, Aug.1986, pp.707-710.
[18] N.O.Sokal & F.H.Raab, "Harmonic output of class-E RF power amplifiers and load coupling network design", IEEE J.Solid-state Circuits, Feb.1977, pp.86-88.
[19] J.Vandelac & P.D.Ziogas, "A novel approach for minimizing high-frequency transformer copper losses", IEEE Trans. Power Electronics, Vol.3, No.3, July 1988, pp.266-276.

```
** CLASS E 48V-5V DC/DC CONVERTER CIRCUIT **
*
VG 20 0 PULSE(0V 10V 500NS 100NS 100NS 400NS 1US)
RG 20 22 5
COX 22 99 2.5NF
DGD 99 10 CDEPL
.MODEL CDEPL D(IS=1E-30 RS=.1 CJO=2.5NF VJ=0.1 FC=.6)
MX 10 22 0 0 MIRF640
.MODEL MIRF640 NMOS(LEVEL=3 GAMMA=0 KAPPA=0
+VTO=3.79 KP=20.7U W=.66 L=2U RDS=889K RD=95.6m RS=19.6m
+RG=2.95 IS=16.4P TT=312N CBD=1.87N CGSO=1.74N)
*
VIN 5 0 PWL(0NS 0V 100NS 48V)
L1 5 10 150UH
C1 10 0 1.1NF
C2 10 30 1.79NF
L2 30 32 15UH
RL2 32 35 .5
LP 35 0 10
LS1 40 0 1
RLS1 40 42 .001
LS2 0 45 1
RLS2 45 47 .001
K12 LP LS1 LS2 .98 K3C8
.MODEL K3C8 CORE(MS=420E3 ALPHA=2E-5 A=26 C=1.05 K=18
+AREA=.635 PATH=3.15 GAP=.1)
D1 42 50 D
.MODEL D D(IS=1E-5 RS=.001 VJ=.75 M=.462 CJO=2.5NF)
D2 47 50 D
COUT 50 0 2.8U
ROUT 50 0 .5
*
.OPTIONS ITL4=40 ITL5=0 RELTOL=.05
.TRAN 10NS 40US 0 30N
.PROBE
.END
```

Appendix A. PSpice listing of a single-ended 48V-5V 50W DC/DC converter operating at 1MHz.

```
** CLASS E PUSH-PULL 48V-5V DC/DC CONVERTER CIRCUIT **
* 500kHz
VG 20 0 PULSE(0V 10V 1uS 50NS 50NS 1uS 2US)
RG 20 22 5
COX 22 99 2.5NF
DGD 99 10 CDEPL
.MODEL CDEPL D(IS=1E-30 RS=.1 CJO=2.5NF VJ=0.1 FC=.6)
MX 10 22 0 0 MIRF640
.MODEL MIRF640 NMOS(LEVEL=3 GAMMA=0 KAPPA=0
+VTO=3.79 KP=20.7U W=.66 L=2U RDS=889K RD=95.6m RS=19.6m
+RG=2.95 IS=16.4P TT=312N CBD=1.87N CGSO=1.74N)
VGA 70 0 PULSE(0V 10V 2US 50NS 50NS 1uS 2US)
RGA 70 72 5
COXA 72 97 2.5NF
DGDA 97 60 CDEPL
MXA 60 72 0 0 MIRF640
*
VIN 5 0 PWL(0NS 0V 100NS 40V)
L1 10 5 150UH
C1 10 0 9NF
L1A 5 60 150UH
C1A 60 0 9NF
C2 10 30 8NF
L2 30 32 15UH
RL2 32 35 .2
LP 35 60 12
LS1 40 0 1
RLS1 40 41 .001
LS2 0 45 1
RLS2 45 46 .001
K12 LP LS1 LS2 .98 K3C8
.MODEL K3C8 CORE(MS=420E3 ALPHA=2E-5 A=26 C=1.05 K=18
+AREA=.635 PATH=3.15 GAP=.12)
D1 41 50 D
.MODEL D D(IS=1E-5 RS=.001 VJ=.75 M=.462 CJO=2.5NF)
D2 46 50 D
COUT 50 0 5U
ROUT 50 0 .125
*
.OPTIONS ITL4=40 ITL5=0 RELTOL=.1
.TRAN 10NS 50US 0 40N
.PROBE
.END
```

Appendix B. PSpice listing of a push-pull 48V-5V 200W DC/DC converter operating at 500kHz.

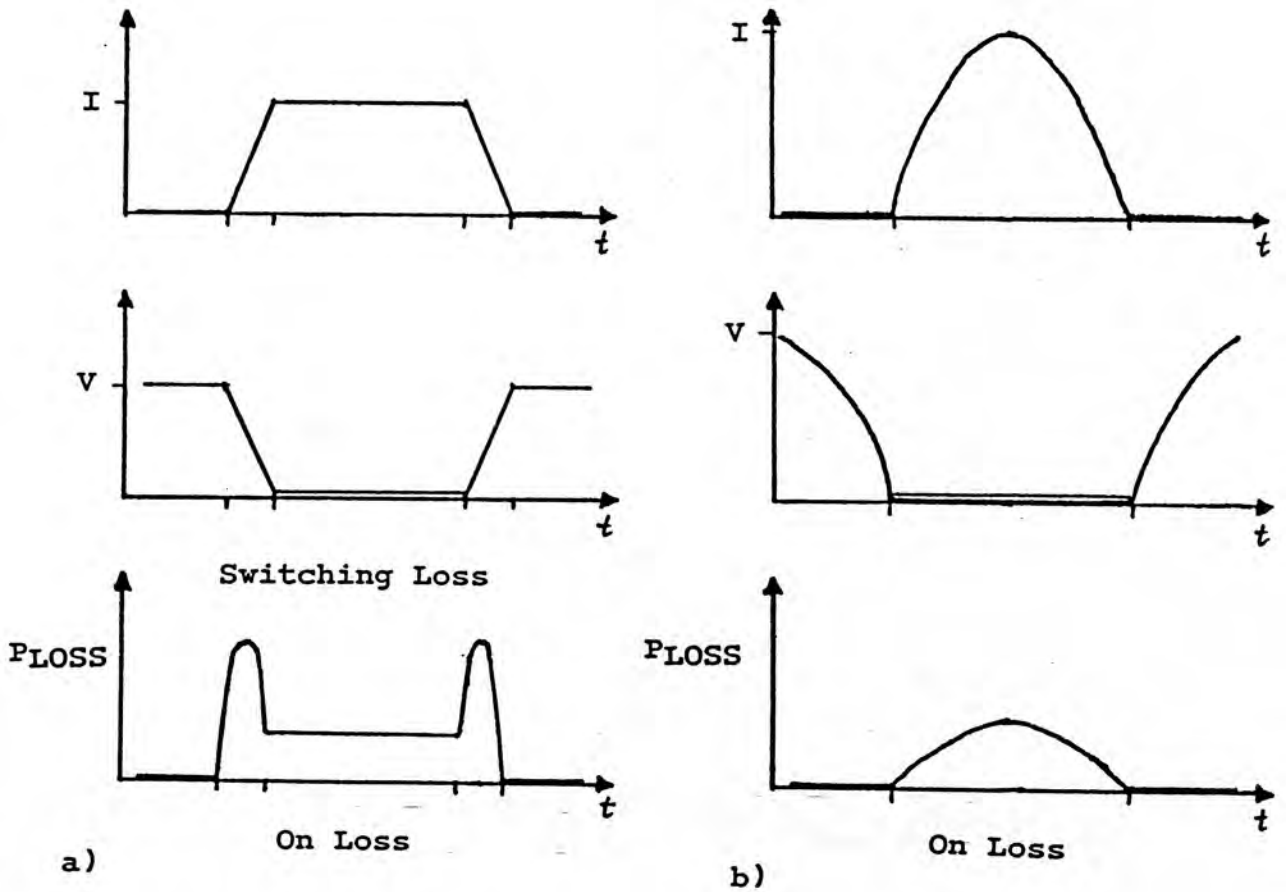


Figure 1. Schematic switch waveforms of voltage, current and power loss in a) square-wave conversion and b) zero-voltage-switched (ZVS) resonant conversion.

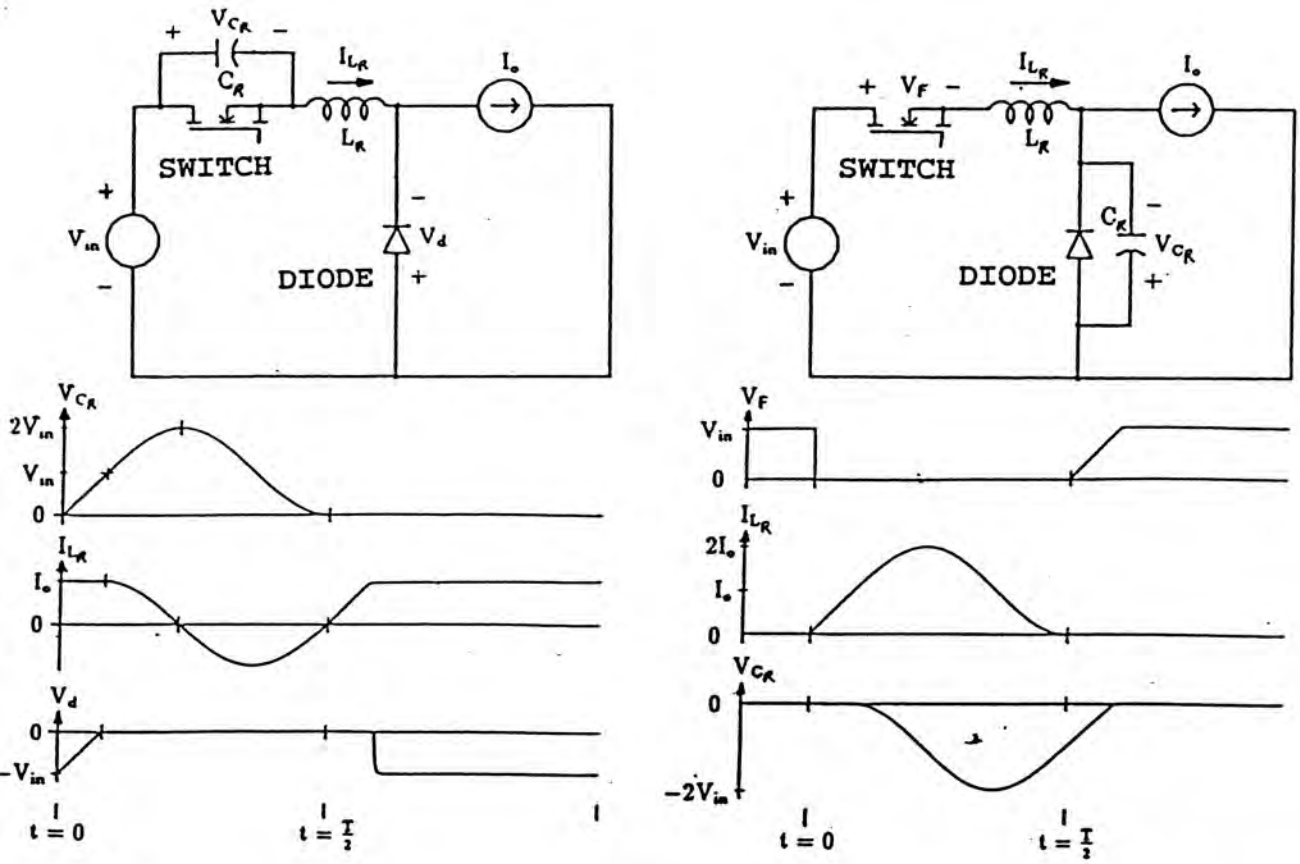


Figure 2. Two quasi-resonant buck converter circuits to provide a) ZVS and b) ZCS.

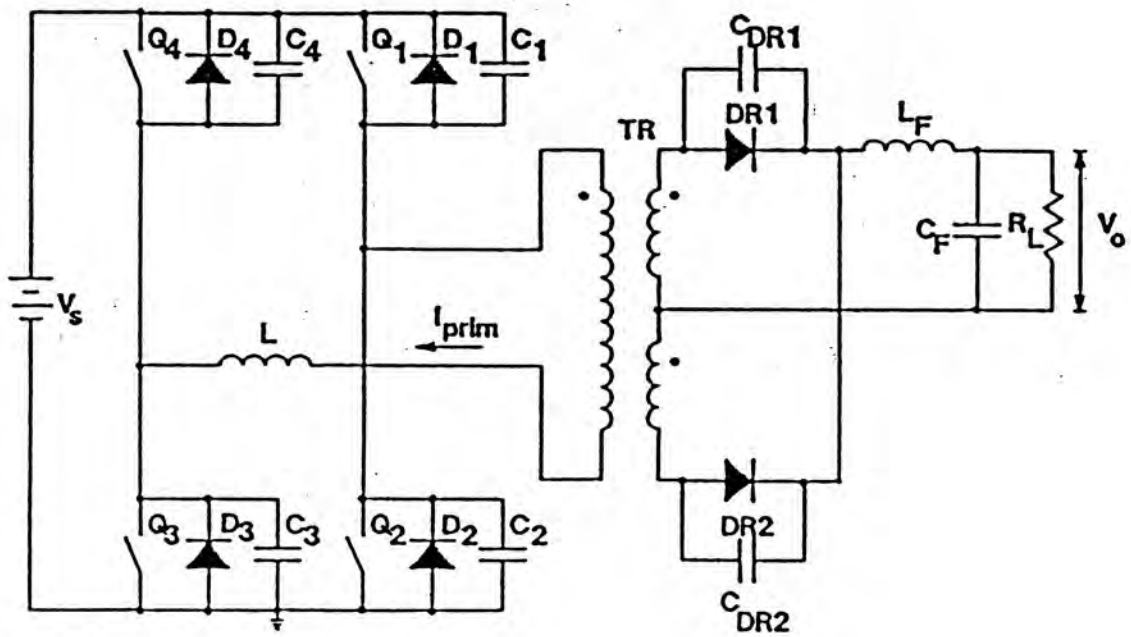


Figure 3. Full-bridge zero-voltage-switched multi-resonant converter (FB-ZVS-MRC).

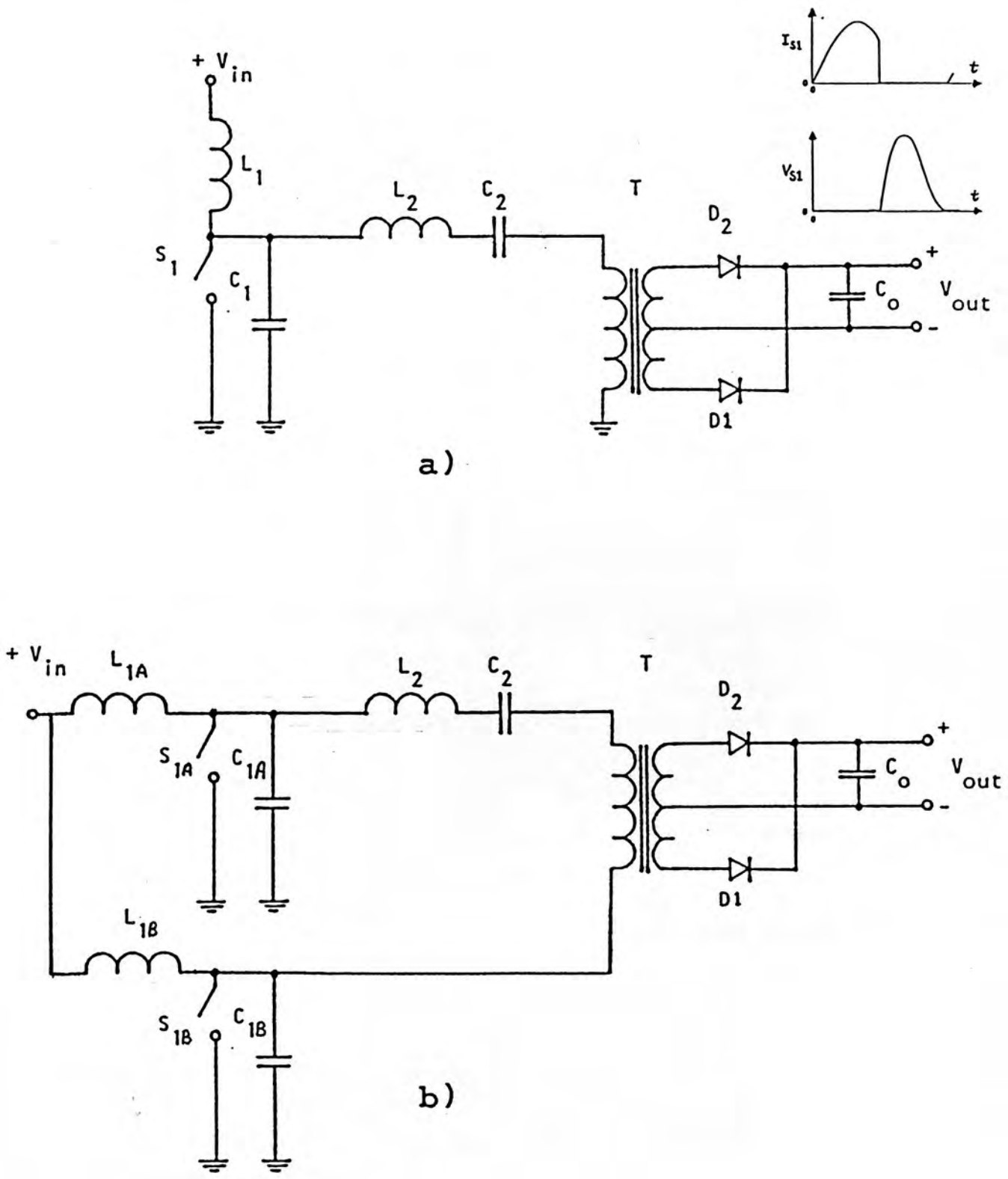


Figure 4. a) Single-ended and b) push-pull Class E converter topologies.

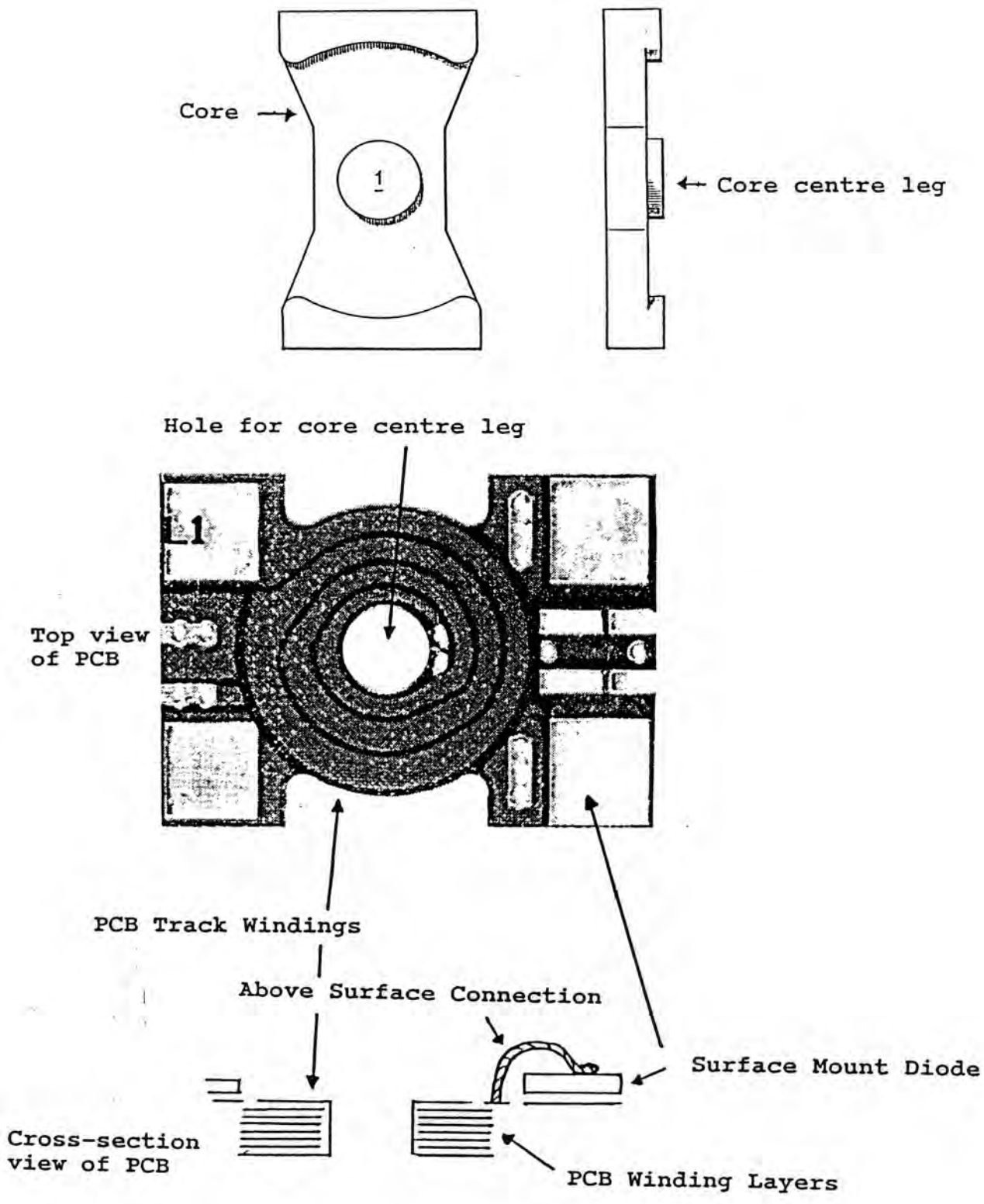


Figure 5. Top and cross-section views of both the core and the Statronics 8 layer PCB. The PCB incorporates the transformer windings and two surface-mount diodes.

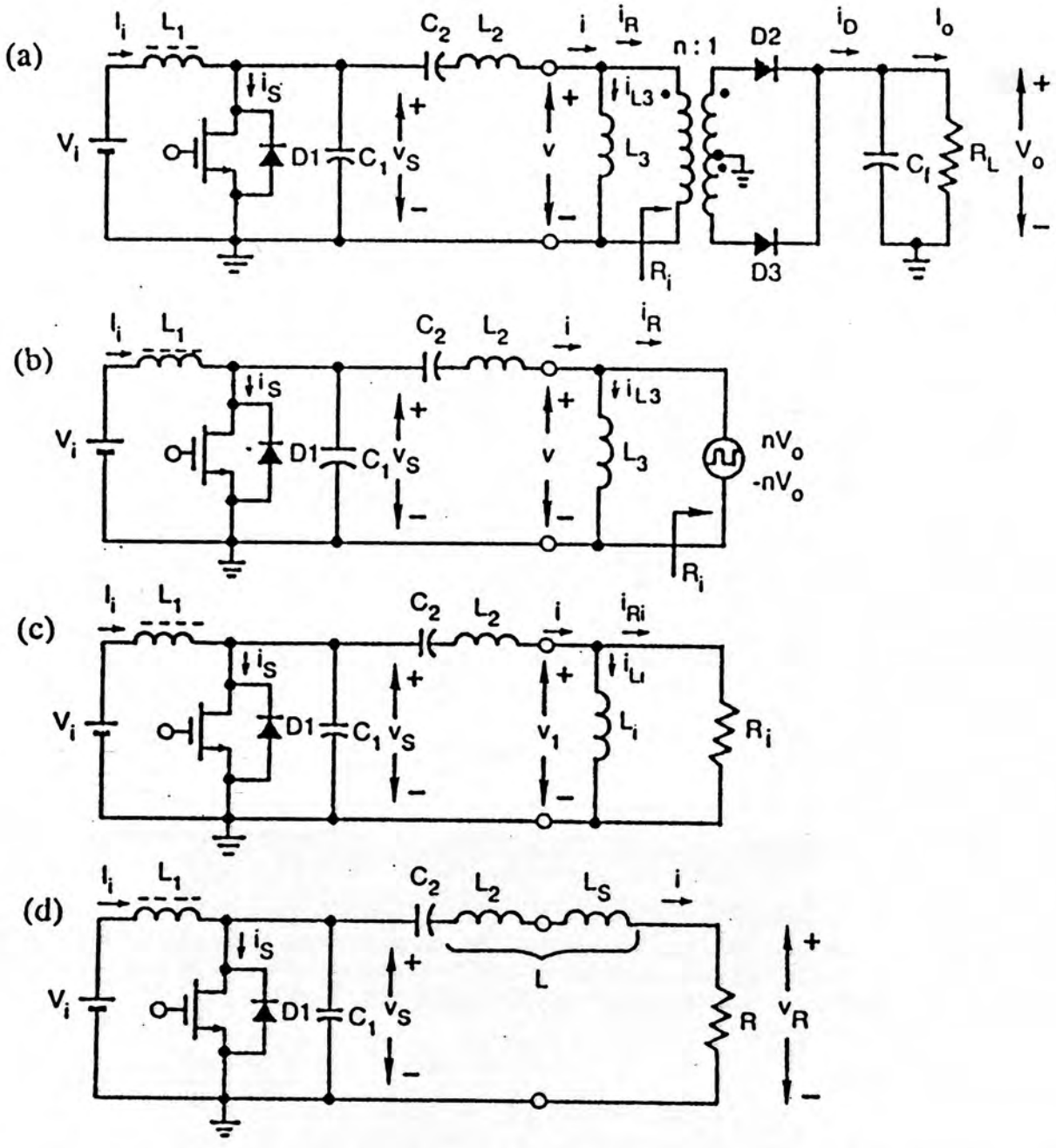


Figure 6. Single-ended Class E DC-DC converter. a) Circuit. b) Equivalent circuit. c) Circuit of Class E inverter with matching network. d) Basic circuit of Class E inverter.

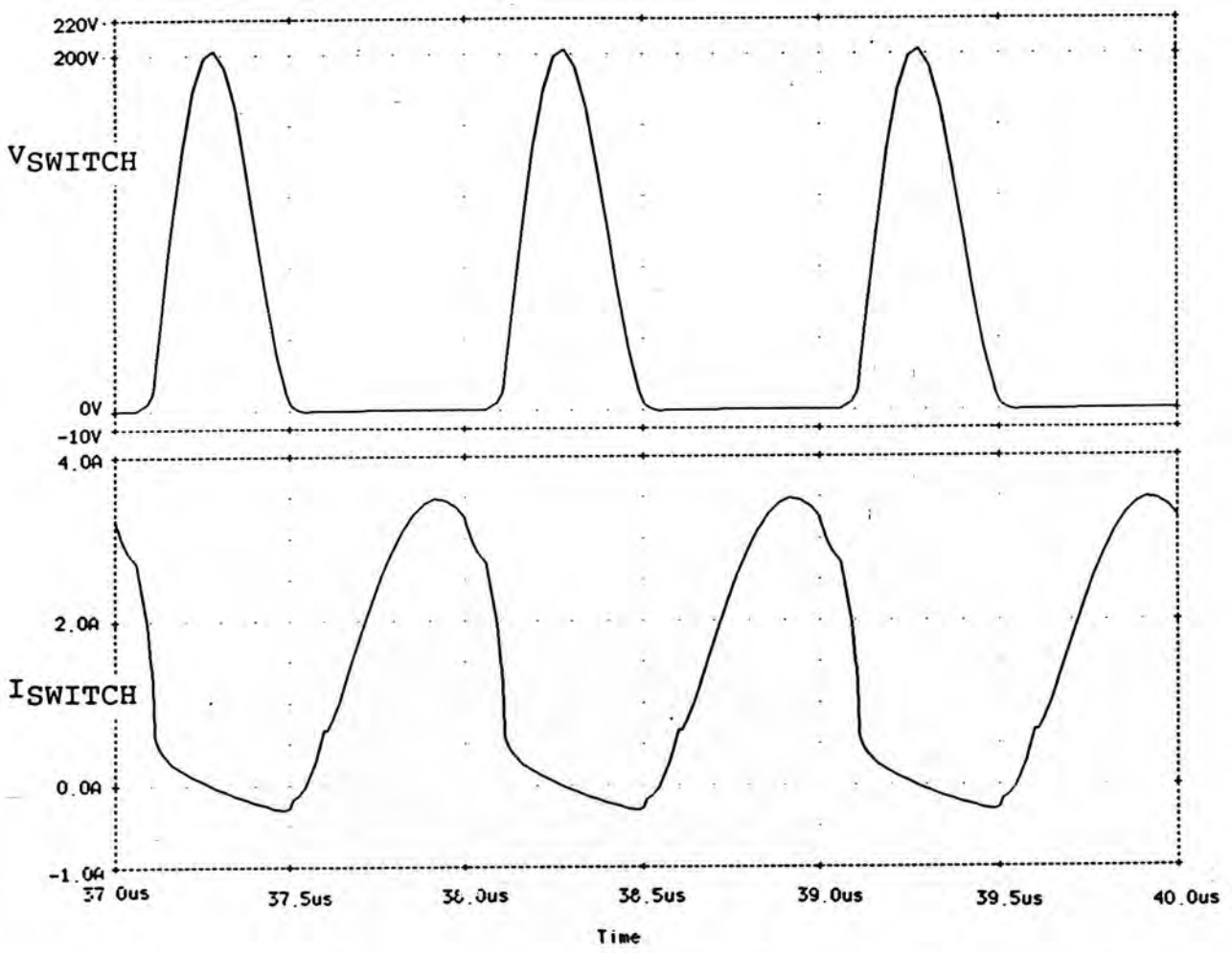


Figure 7. Simulated switch voltage and current waveforms in a single-ended 50W Class E converter showing ZCS at turn-on and ZVS at both turn-on and turn-off.

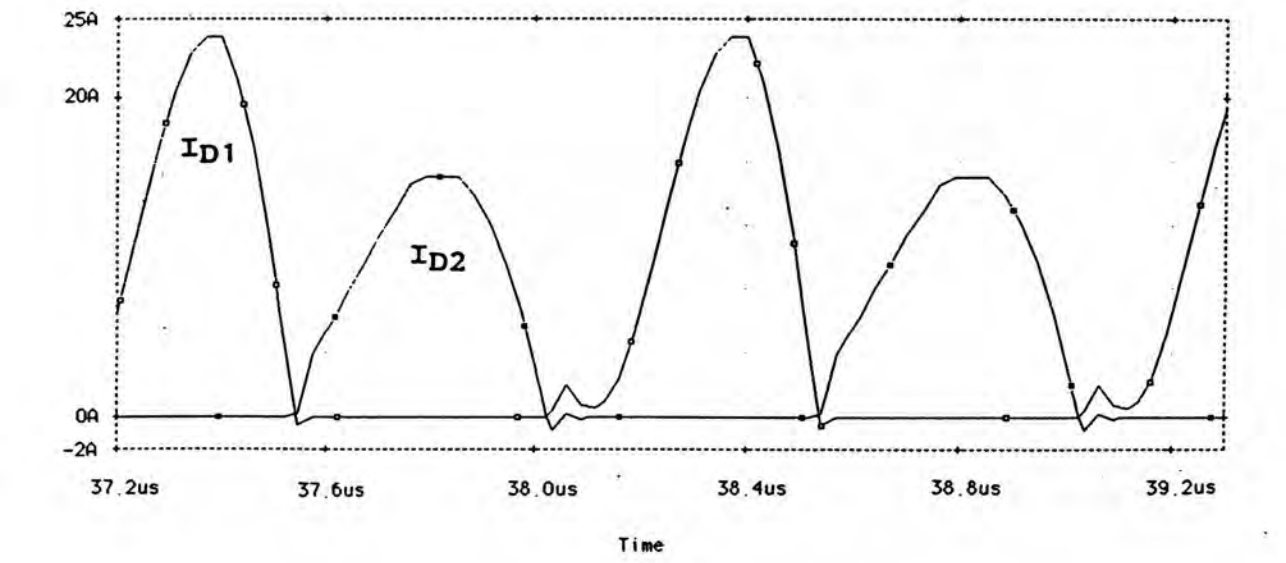
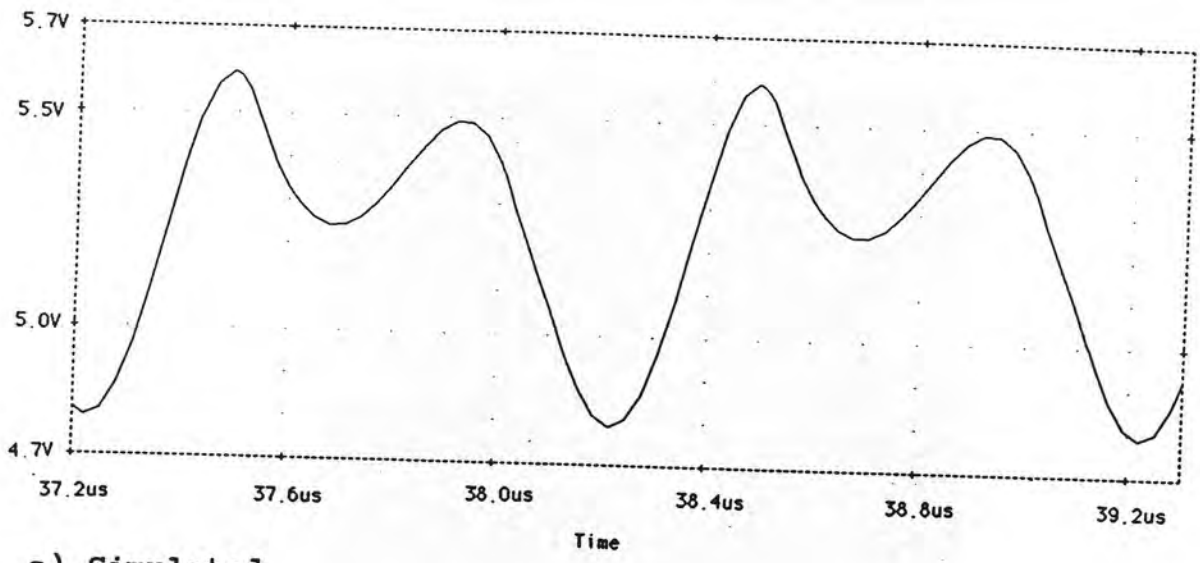
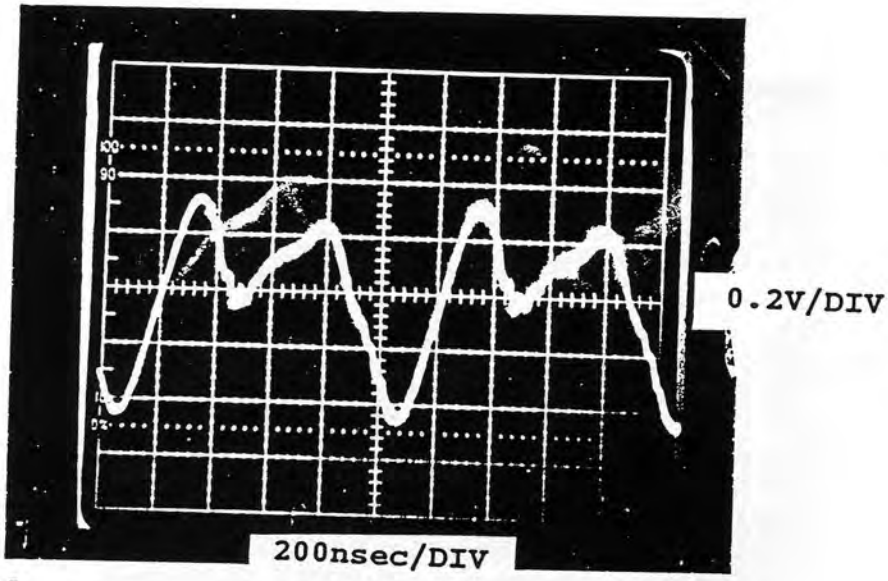


Figure 8. Simulated rectifier diode current waveforms in a single-ended 50W Class E converter showing current asymmetry between I_{D1} and I_{D2}.

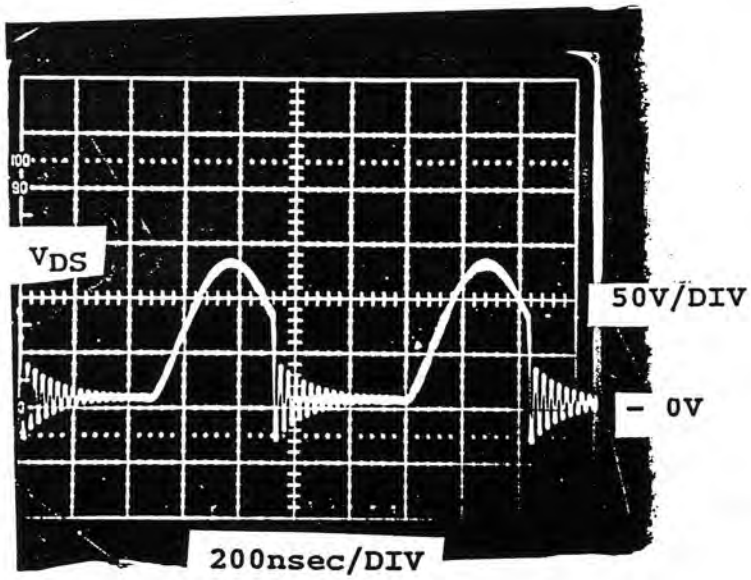


a) Simulated

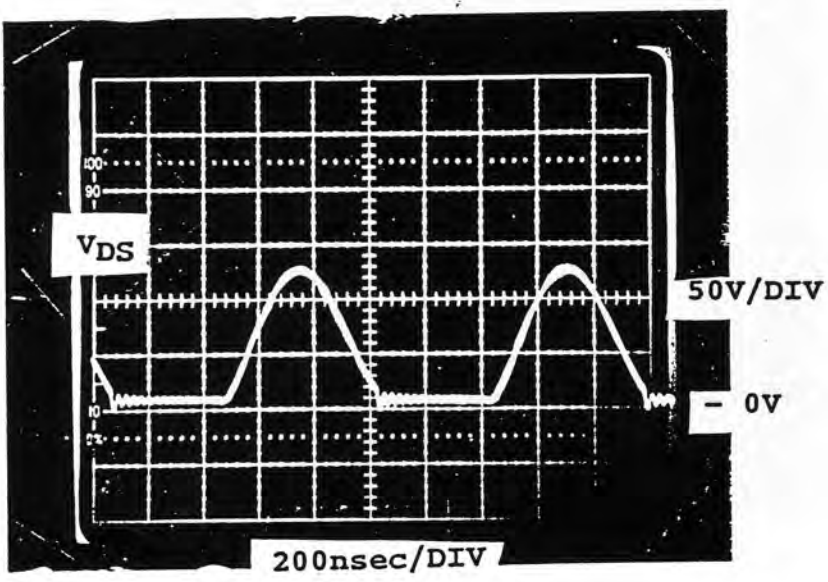


b) Measured

Figure 9. a) Simulated and b) measured output voltage ripple waveforms in a single-ended 50W Class E converter showing distorted sinusoid shape caused by diode current asymmetry.



a) Frequency control: f= 1.095 MHz, duty-cycle= 0.50, P_{IN}= 11.6W.



b) Frequency and duty-cycle control: f= 1.050 MHz, duty-cycle= 0.41, P_{IN}= 4.3W.

Figure 10. Measured switch voltage waveforms in a single-ended Class E converter at 5V, 2.5W output (5% of full load) with a) frequency control only, and b) frequency and duty-cycle control.

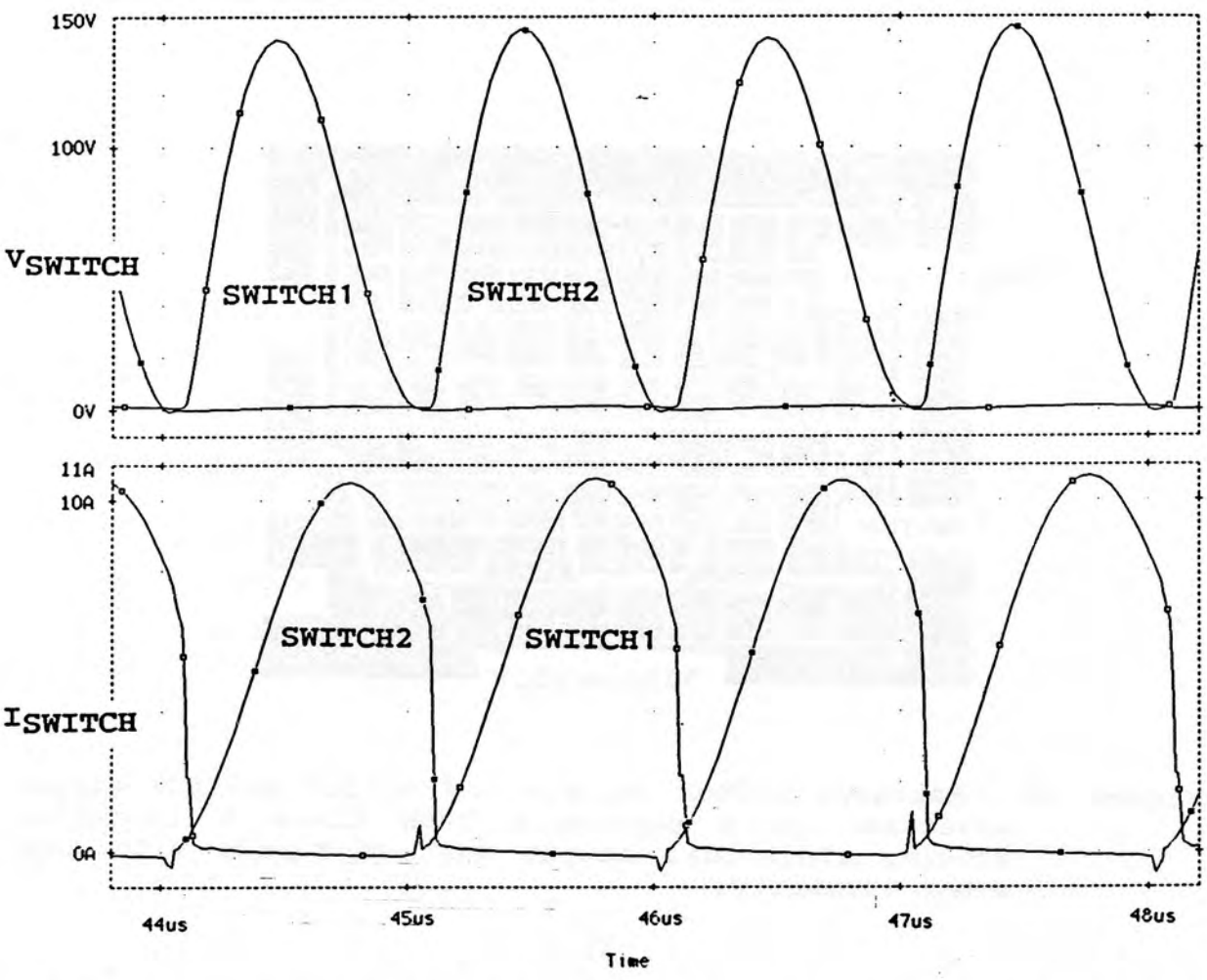


Figure 11. Simulated voltage and current waveforms for both switches in a push-pull 200W Class E converter showing ZCS at turn-on and ZVS at both turn-on and turn-off.

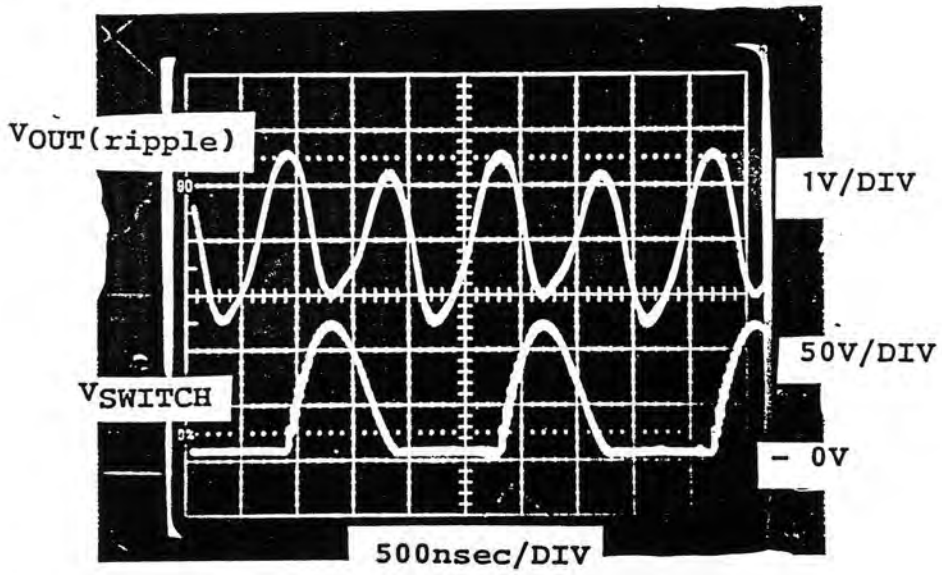


Figure 12. Measured switch voltage and output voltage ripple waveforms in a push-pull 200W Class E converter showing sinusoidal output voltage ripple with only minor asymmetry.

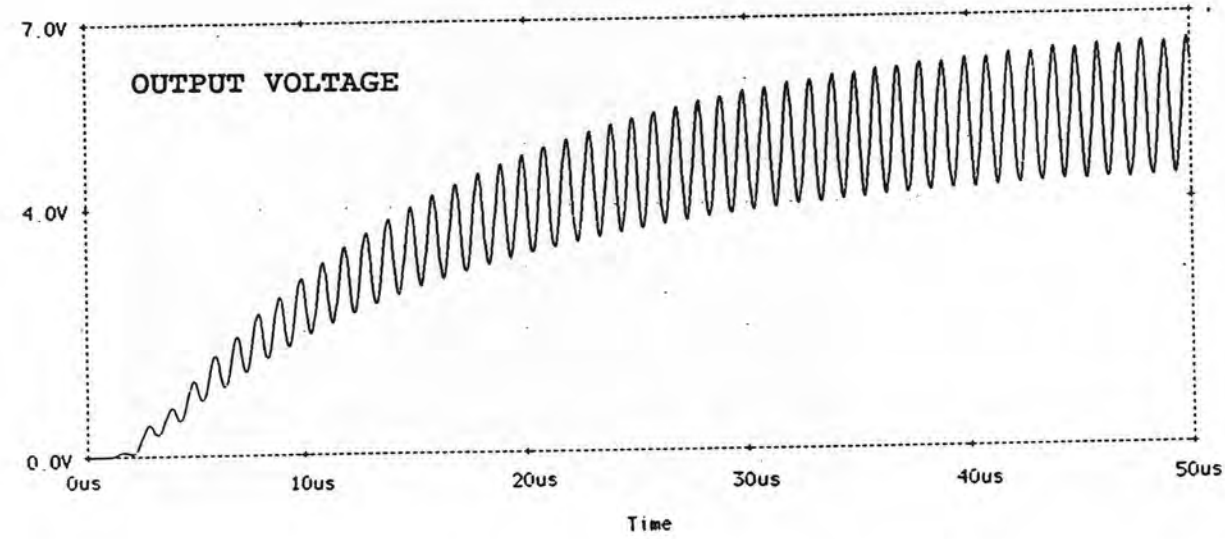


Figure 13. Simulated output voltage of a push-pull 200W Class E converter during the first 25 cycles after power-on.